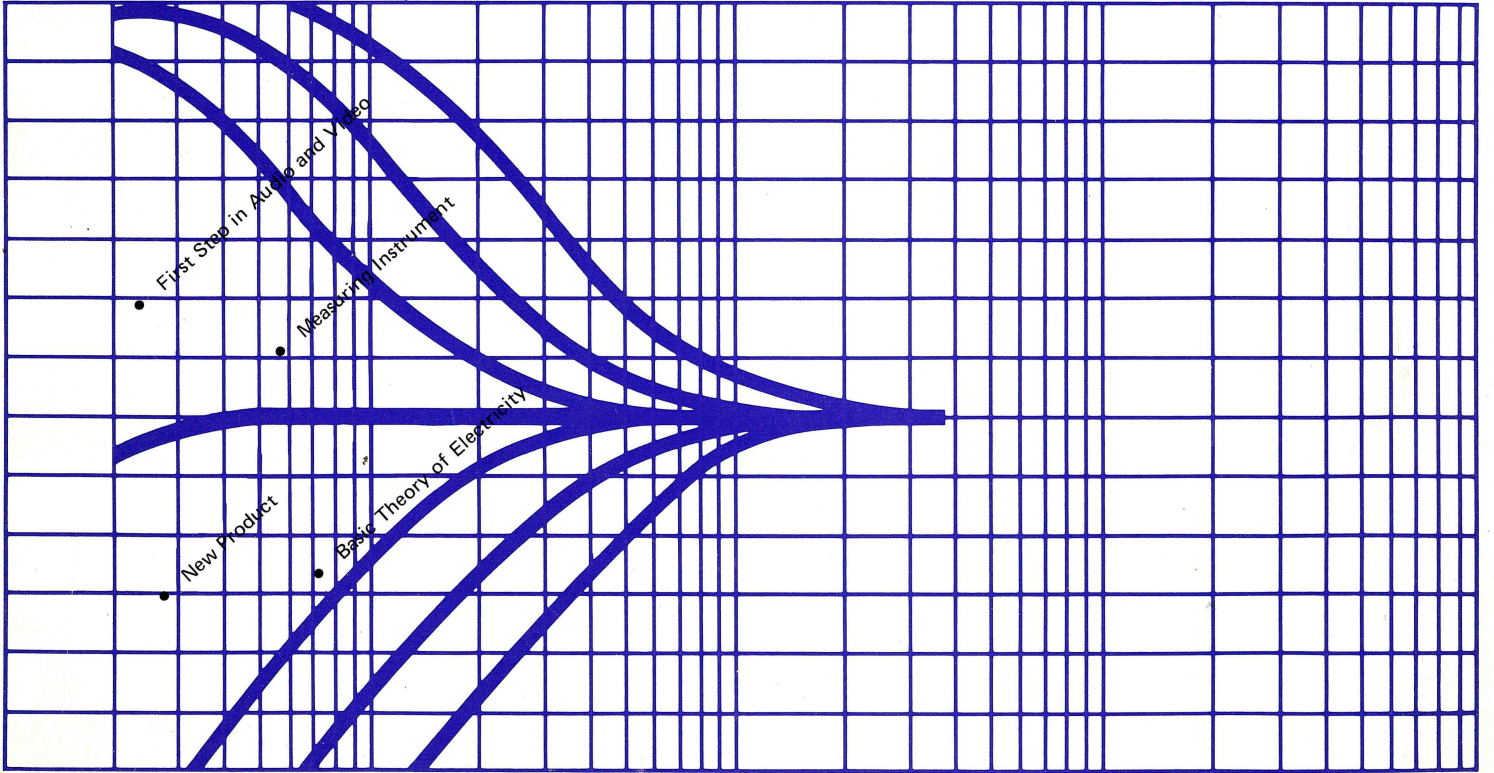


TUNING FORK

Audio and Video Service Guide

No. 7



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Parts Information

Display Devices

A display device provides us with various information visually in the form of characters, symbols, figures or pictographs. Recently, various display devices have been employed in audio and video equipment such as CRT (cathode-ray tube), frequency displays for tuners, receivers, and car stereos that employ quartz phase-locked loop

(PLL) synthesizers; electronic counters for tape decks; and time indicators for clocks. Let's discuss three devices here: the LED (light-emitting diode), fluorescent lamp (FL), and liquid crystal display (LCD). We shall describe their structure, features, and performance. Features are compared in table.

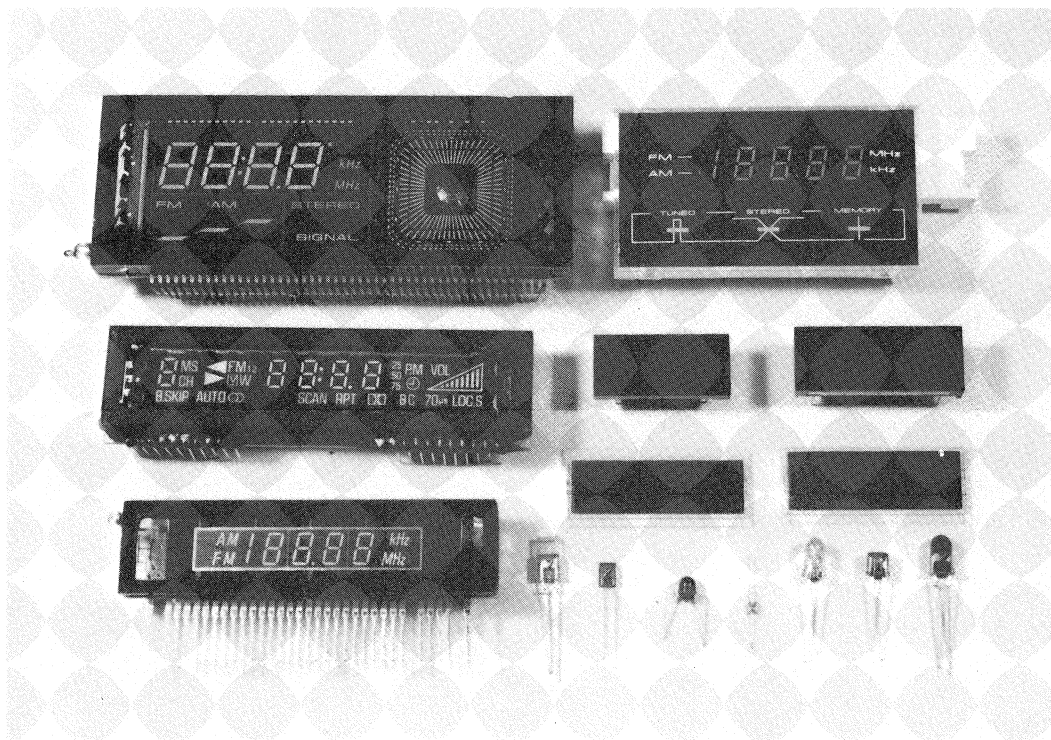


Photo 1. Display Devices Used in Pioneer Products

	LED	FL	LCD
Power consumption	Fair	Good	Excellent
Operating voltage	Excellent	Good	Excellent
Service life	Excellent	Excellent	Excellent
Allowable temperature	Excellent	Excellent	Fair
Response speed	Excellent	Excellent	Fair
Brightness	Good	Excellent	Good
Contrast	Fair	Good	Fair
Shock resistance	Excellent	Good	Good

Table 1. Features of LEDs, FLs, and LCDs

1. LED

An LED is luminous diode that has a PN junction that emits light when it is forward biased.

1.1 Structure and Shape

There are two kinds of LED. One is the LED lamp and the other is the LED display (integrated LED).

a) LED lamp

A typical LED lamp can be made by mounting a small LED chip on a frame lead and molding it in a transparent or light-diffusing resin as illustrated in Fig. 1.

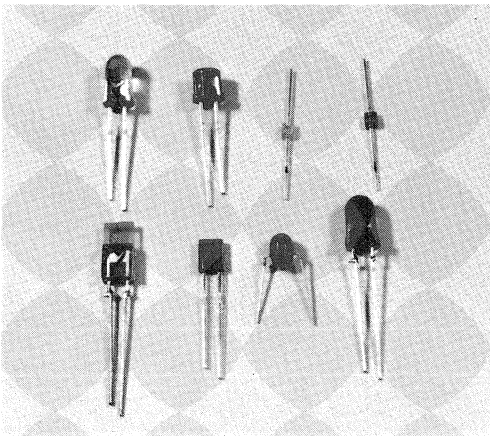


Photo 2 LED Lamps Used in Pioneer Products

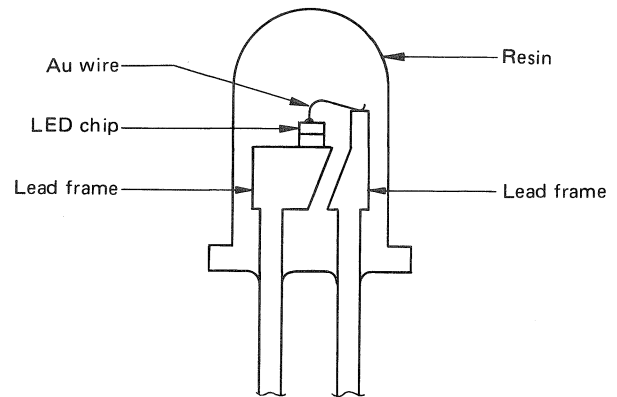


Fig. 1 Structure of an LED

To distinguish between cathode and anode electrodes, the cathode lead is given one of the following treatments, as shown in Fig. 2:

- Trimming
- Painting
- Making a larger stopper
- Others

Please note that in a very few cases, the above treatments are applied to the anode lead instead of the cathode lead.

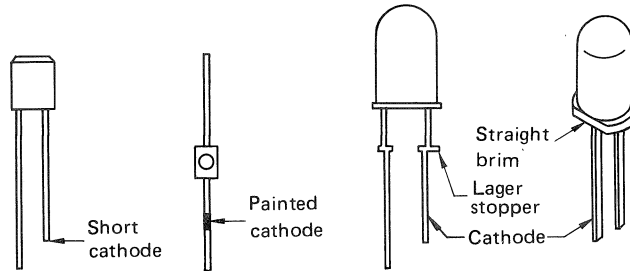


Fig. 2 Distributing Cathode

b) LED display

An LED display is made of several LED chips bonded on a printed-circuit board (PCB). The arrangement depends on the shape of the character or figure to be displayed. Fig. 3 shows the structure of an LED display.

The foil pattern of the PCB is gilded to facilitate wire-bonding. Highly reflective resin is used for the reflector to illuminate the desired area evenly and efficiently. The diffuser evens the brightness by diffusing both direct and reflected light. The screen is used for making clear-cut figures. Photo 3 shows an exploded view of an LED display (CWW-189).

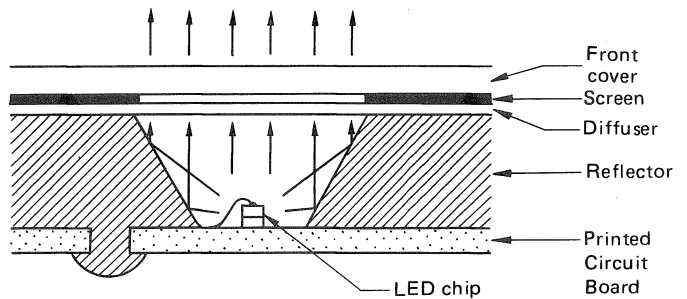


Fig. 3 Structure of LED Display

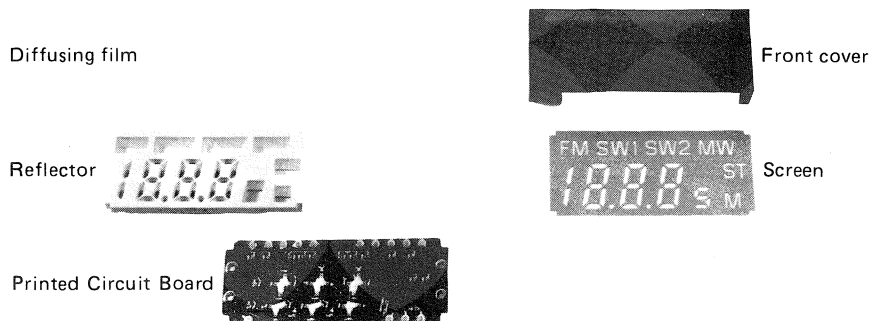


Photo 3 LED Display CWW-189

There are two internal connection methods for LED displays, anode common and cathode common, as illustrated in Fig. 4.

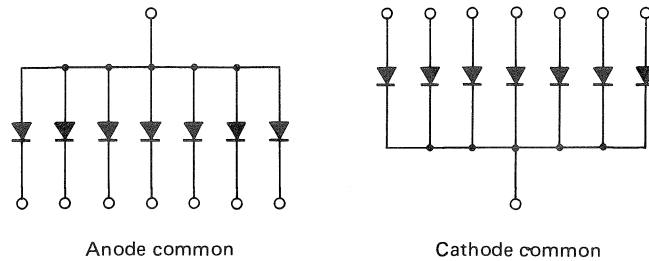


Fig. 4 Internal connection of LED

1.2 Characteristics of LED

a) Forward voltage (V_F) and forward current (I_F)

Fig. 5 illustrates the characteristic of forward current (I_F) vs voltage (V_F). An LED has the same property as that of an ordinary diode. V_F depends on the material of the crystal in the chip and the construction of the frame lead. Fig. 6 shows the relationship of allowable I_F to ambient temperature (T_a). Allowable I_F decreases as ambient temperature increases. Because current generates heat, excessive current shortens the diode's service life. In driving LEDs, a forward pulse current (I_{FP}) is more effective than a DC because the lower the duty ratio, the lower the power consumption.

b) Reverse voltage (V_R) and reverse current (I_R)

A special PN junction is required to emit light. To make

a high reverse voltage (V_R) diode, it is necessary to change the quantity of additives in the PN junction. It is impossible, however, to change the quantity of additives enough to maintain efficient light emission. High- V_R LEDs are therefore not available at present. LEDs on the market have V_R ratings from 3 to 15 volts, but mostly in the 3- to 5- volt range. In design of LED circuits, reverse biasing should be avoided.

c) Relative luminous intensity and forward current (I_F)

Fig. 7 shows the characteristic of relative luminous intensity vs forward current (I_F). Relative luminous intensity is the ratio of the intensity of an LED to a reference intensity that is measured at an ambient temperature of 25°C with the rated forward current applied to the LED. Intensity is proportional to I_F .

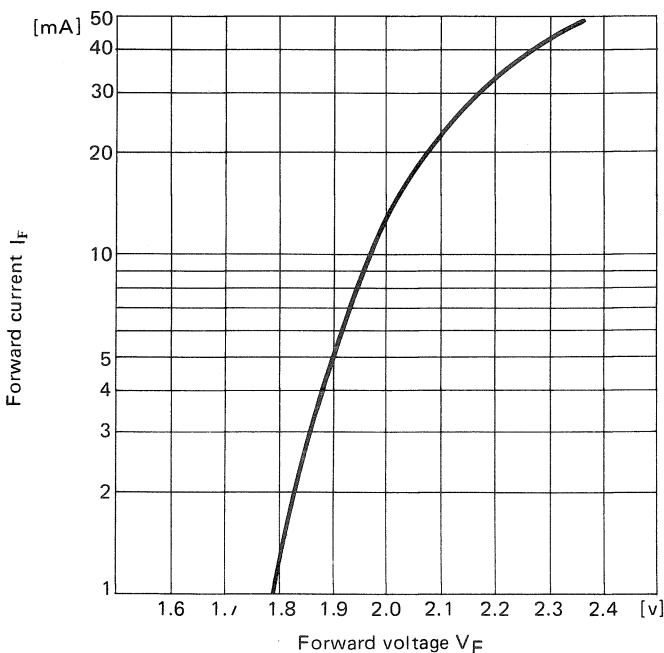


Fig. 5 Forward Current vs. Voltage

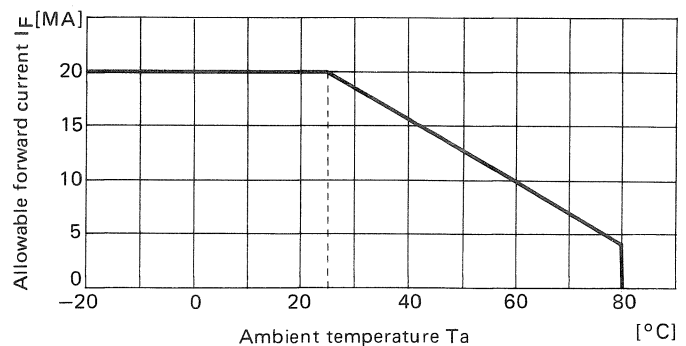


Fig. 6 Forward Current vs. Temperature

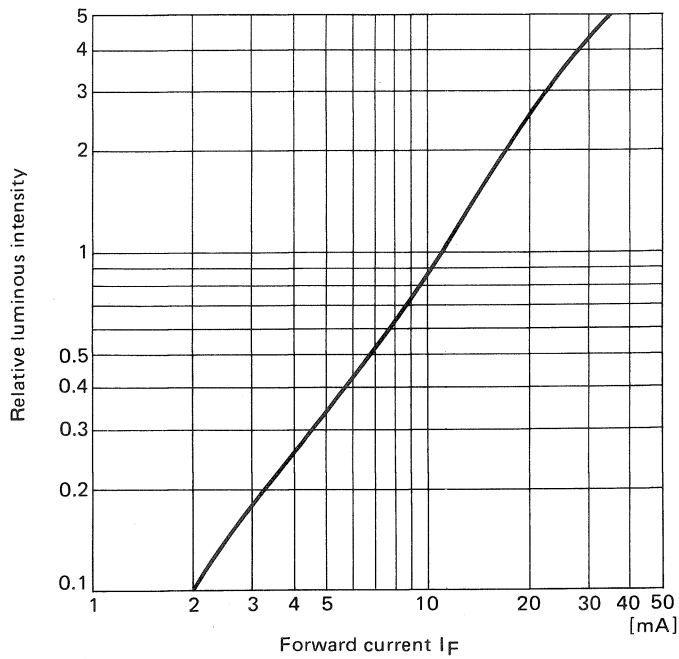


Fig. 7 Relative Luminous Intensity vs. Forward Current (I_F)

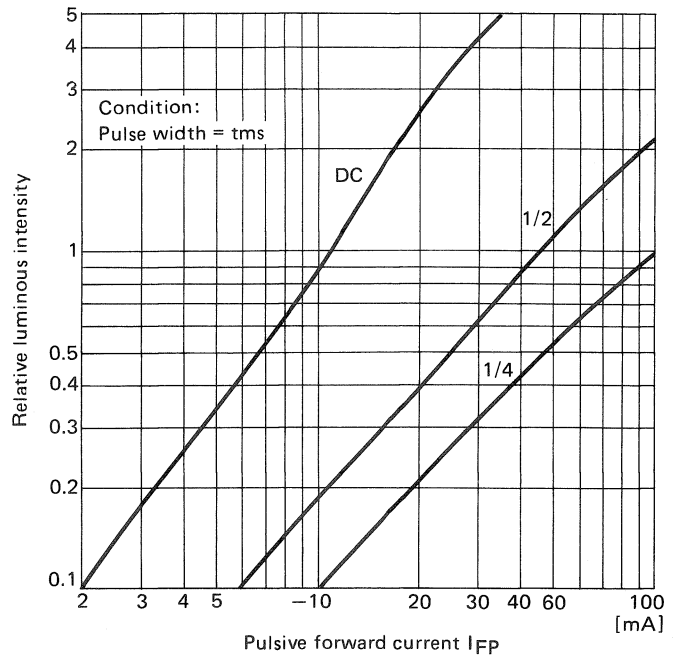


Fig. 8 Relative Luminous Intensity vs. Pulse Forward Current (I_{FP})

Fig. 8 shows the relationship between relative luminous intensity and I_{FP} . Two figures can be dynamically displayed with a pulse current at 50% duty factor, and four figures can be displayed at 25% duty factor, by timesharing.

d) Relative luminous intensity and ambient temperature (T_a)

Fig. 9 shows the relationship between relative luminous intensity and ambient temperature (T_a). The higher the temperature, the lower the luminous intensity.

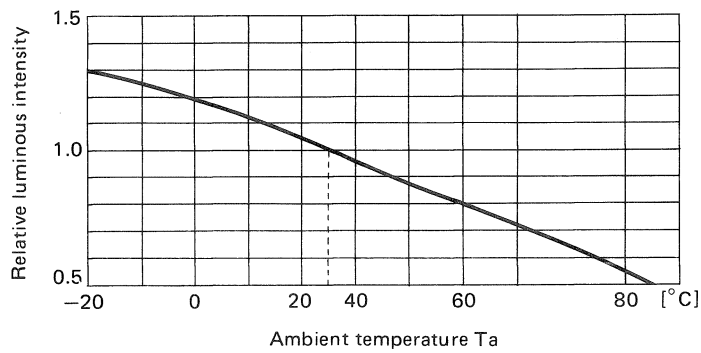


Fig. 9 Relative Luminous Intensity vs. Ambient Temperature (T_a)

e) Luminescence spectrum of LED

Fig. 10 shows the luminescence spectra of three LEDs. The wavelength at peak luminescence and bandwidth of the curve depend on the crystal material and additives in the chip.

Color	LED/Base
Red	GaAs _{0.6} P _{0.4} /GaAs GaP:ZnO/GaP
Vermillion	GaAs _{0.35} P _{0.85} /GaP
Yellow	GaAs _{0.15} P _{0.85} /GaP
Green	GaP:N/GaP GaP/GaP
Blue	GaN/Al ₂ O ₃

Table 2 Luminant Color and Base Materials

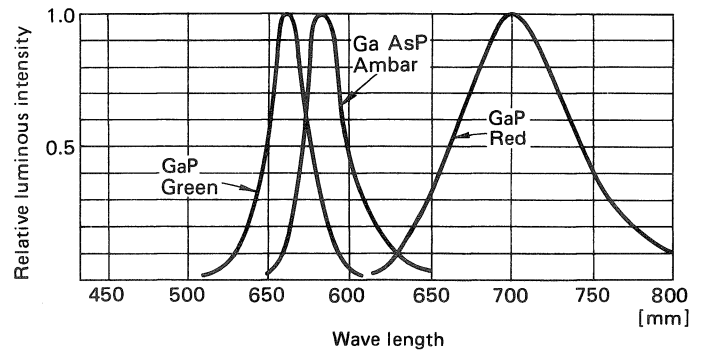


Fig. 10 Luminescence Spectra of LEDs

f) Luminous efficiency

Luminous efficiency is the ratio of luminous flux to radiant flux. It depends on luminous materials and forward current (I_f). In Fig. 11, a GaP LED (red) becomes bright-

est at a small current. A small DC current is thus suitable for driving GaP LEDs (red), and a pulse current is suitable for the other two types, which are not affected by current variation.

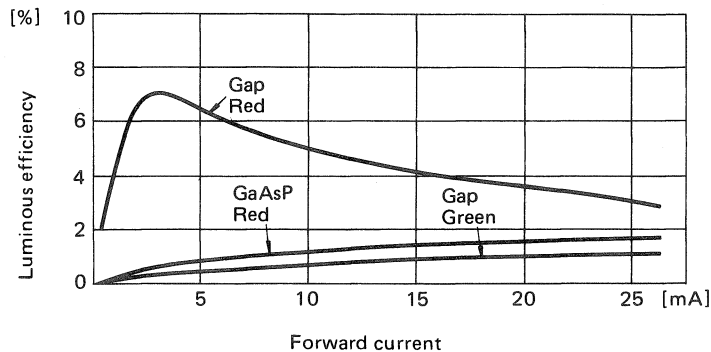


Fig. 11 Luminous Efficiency vs. Forward Current (I_f)

1.3 Drive Circuit

A basic drive circuit is shown in Fig. 12. The circuit is a simple switching circuit. Brightness of an LED is adjustable by changing the forward current (I_F) which is determined by a resistor (R). A driver IC is required for an LED display because every element requires a transistor.

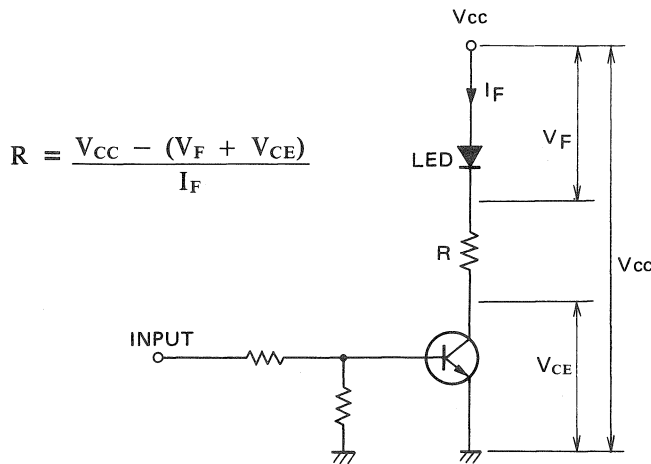


Fig. 12 LED Drive Circuit

2. Fluorescent Tube (display)

An FL is a vacuum tube that emits light. In a vacuum tube, thermoelectrons emitted from the cathode bombard fluorescent materials on the anode, activating those materials.

2.1 Structure and Features of FLs

Fig. 13 shows the basic structure of FLs. Their construction is equivalent to that of a direct-heated triode tube. An FL consists of fine filaments (cathode), meshed grids, and anodes coated with the fluorescent material.

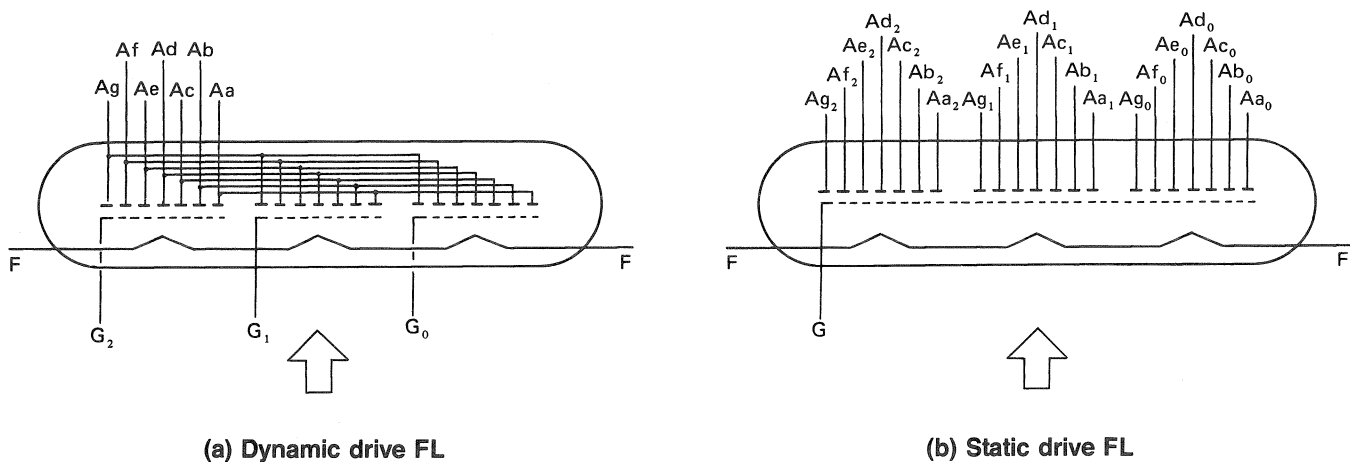


Fig. 13 Structure of FL

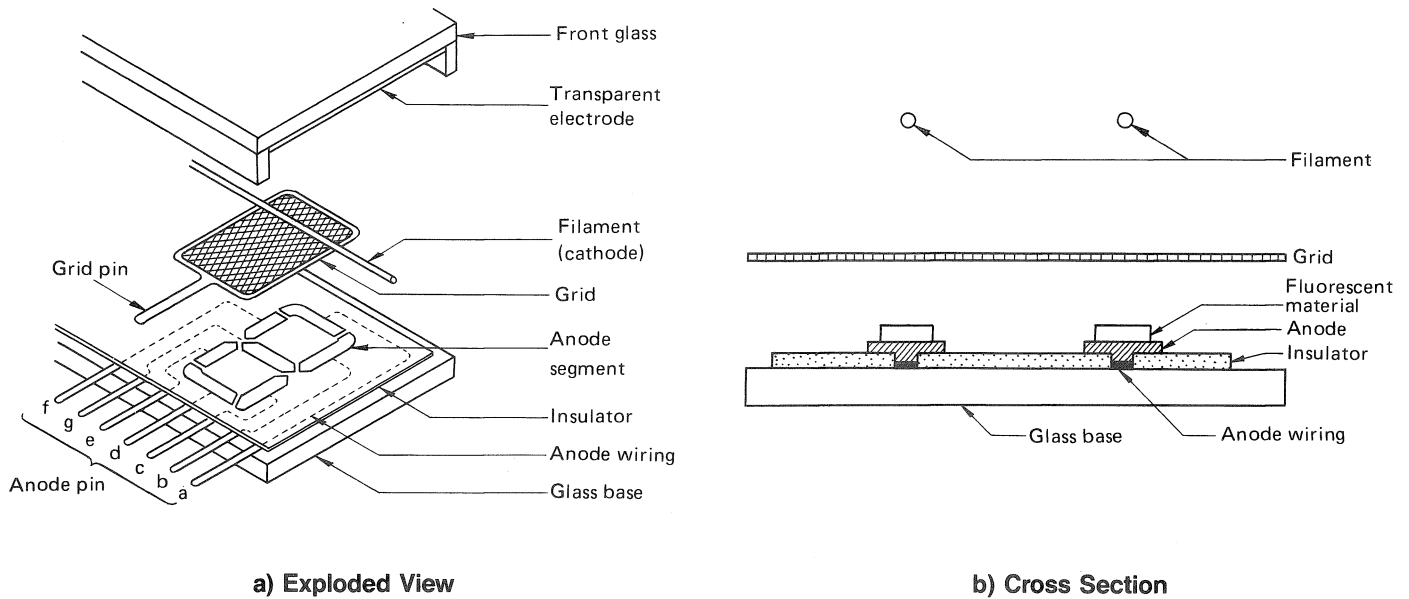


Fig. 14 Structure of an FL

Fig. 14 shows the cross section of an FL. The filament is made of thin, oxide-coated tungsten wire ($\phi 5$ to $\phi 10s \mu m$), and the grid is a thin mesh of stainless steel a few micrometers thick to avoid interfering with the light. When a voltage is applied, the filament is heated to $600^{\circ}C$ and radiates thermoelectrons. Usually a positive voltage is applied to the grid to accelerate the flow of thermoelectrons to the anode. The grid controls the electrons, diffusing them evenly. The anode is a fluorescent film formed into a pattern

on a glass base. The pattern to be displayed is determined by the voltage distribution to anodes and grids. An anode luminesces only when a voltage is applied to both the anode and the grid. Even if the potential at the anode or grid drops, the anode will luminesce if the initial velocity of the thermoelectrons is high and the potential at the directly heated filament drops. So a negative voltage is applied to the anodes or grids of mounted segments to completely turn them off.

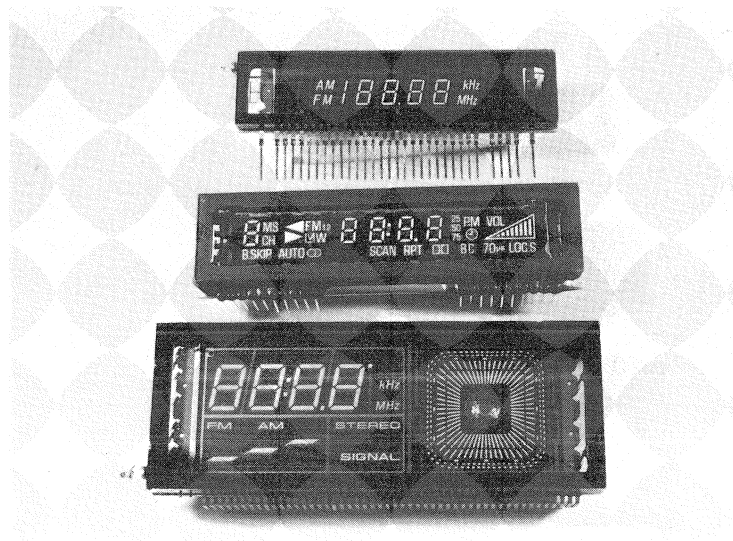


Photo 4 FL displays

2.2 Characteristics of FL

a) Filament current

Either DC or AC could be used for heating the filament. DC is not used, however, because the filament elements are connected in series, and DC voltage decreases every time the current flows through an element; brightness would therefore differ between the right and left figures. Excessive filament voltage (E_f) evaporates the oxide coating on the tungsten wire and damages the filament, whereas insufficient E_f cannot heat the filament and thus, keeps the anode dark. Fluctuation of E_f around the threshold level makes the luminance unstable. Fig. 16 shows the relationship between the filament current (I_f) and voltage (E_f). ↗

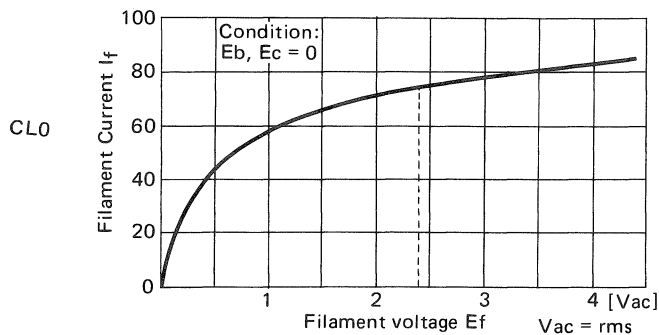


Fig. 15 Filament Current (I_f) vs. Filament Voltage (E_f)

c) Relative brightness and anode/grid voltage

Fig. 17 shows the characteristic of relative brightness to anode and grid voltages. Usually equal positive voltages are fed to the anode and cathode. Brightness is proportional to the 2.5th to 3rd power of the anode and cathode voltage. Fig. 18 shows the characteristic of relative brightness vs duty factor when an FL is driven by a pulse current.

b) Relative brightness vs filament voltage (E_f)

The source of LED light can be considered to be a point, whereas that of an FL is an area. Brightness is the luminous intensity of light emitted from a limited area. Fig. 16 shows the relationship between relative brightness and filament voltage (E_f). The brightness saturates when E_f is increased and rapidly decreases when E_f is decreased. The rated filament voltage is set at a point a little below the saturating point.

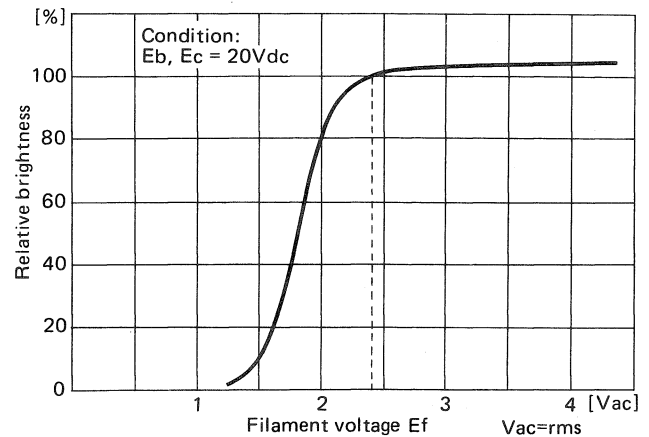


Fig. 16 Relative Brightness vs. Filament Voltage (E_f)

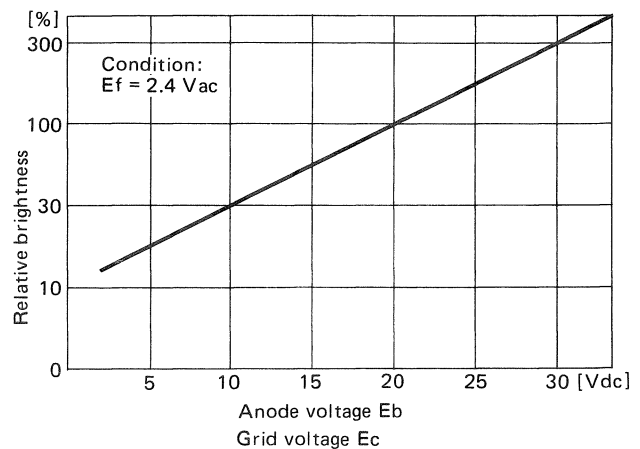


Fig. 17 Characteristic of Relative Brightness vs. Anode and Grid Voltage

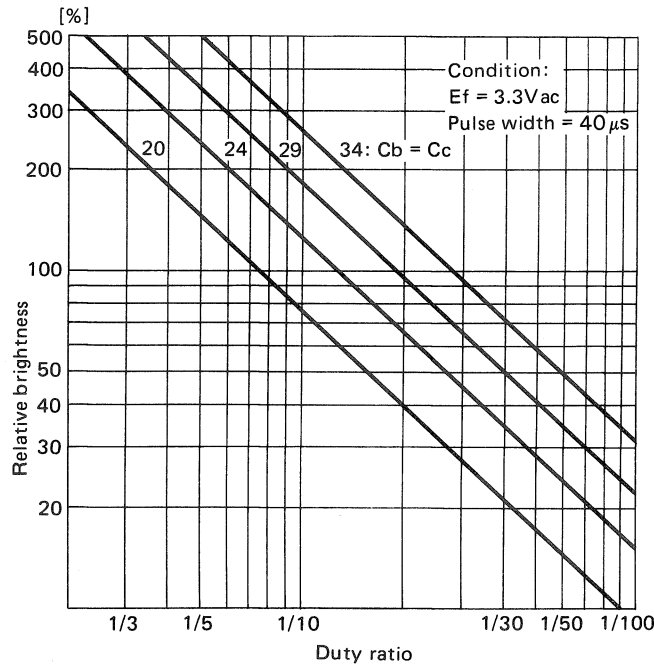


Fig. 18 Characteristic of Relative Brightness vs. Duty Factor

d) Relative brightness and ambient temperature

Fig. 19 shows the relationship between relative brightness and ambient temperature. An FL is bright at low temperatures.

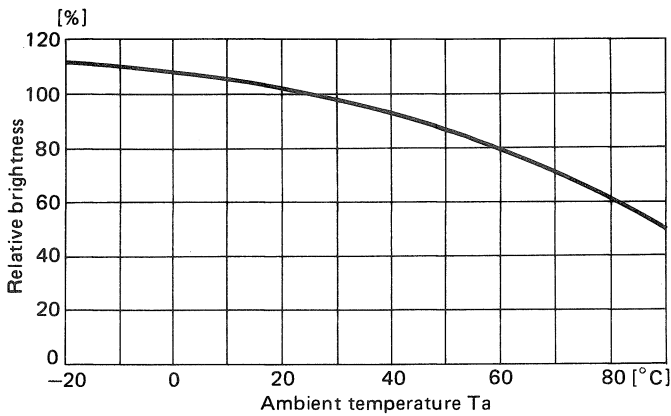


Fig. 19 Relative Brightness vs. Ambient Temperature

e) Spectrum of FL

The color of an FL depends on the fluorescent materials. Green and blue luminant materials especially, zincite (ZnO) are most commonly used because of their visibility. Fig. 20 shows the spectrum of a fluorescent light. An FL causes less fatigue to the human eye than an LED does because the spectrum of an FL is similar to the sensitivity spectrum of the eye, and the spectrum bandwidth of an FL is wider than that of an LED.

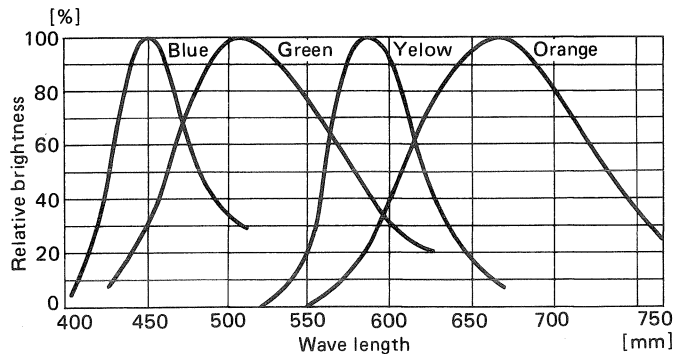


Fig. 20 Spectrum of an FL

f) Cutoff characteristic

As explained in section 2.1 Structure and Features of FLs, it is necessary to apply a negative cutoff voltage to the anode or grid. Generally, the static driving system cuts off the anode, and the dynamic driving system cuts off the grid. Fig. 21 shows the grid cutoff characteristics.

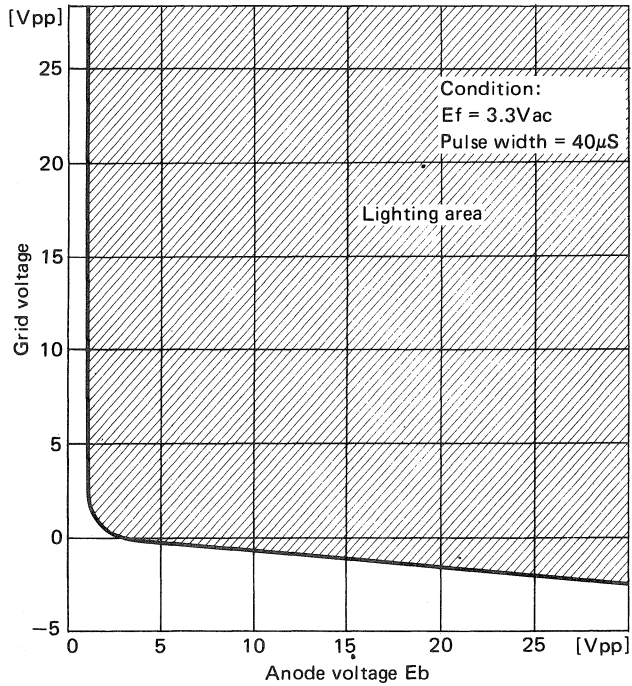


Fig. 21 Anode/grid Cutoff Characteristic

2.3 Drive Circuit

Fig. 23 shows a basic drive circuit for an FL. The filament (cathode) radiates thermoelectrons when heated. When the input levels are H, Q1 and Q3 turn on. Currents flow through R3 and R7, V_{EB} of Q2 and Q4 goes to 0.6V. Q2 and Q4 turn on, and +20 V is applied to the anode and grid. The FL turns on. When the input levels are low, all transistors (Q1 to Q4) are off, the anode and cathode are

g) Response time of fluorescent materials to a pulse

The response time of fluorescent materials affects the quality of the display. Fig. 22 shows the luminous response of fluorescent materials to a pulse applied to the anode and grid. Rise time (t_r) and fall time (t_f) of the brightness are 10 s each. It is necessary to make the pulse width and pulse interval wider than t_r and t_f respectively.

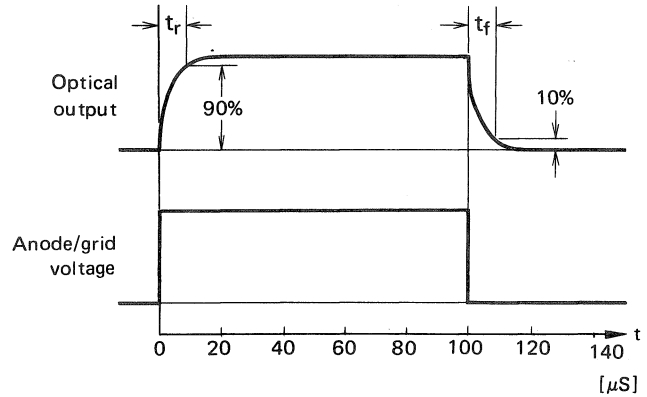


Fig. 22 Luminous Response of a Fluorescent Material vs. Pulse Signal

grounded through pull-down resistors (R4 and R8), and the FL is off. A +5 V level is applied to the center tap of the transformer secondary winding to supply the FL with a reverse bias that turns it off completely when the inputs are L. In multi-figure displays, the drive circuit is usually integrated into an IC because the number of anodes and grids is very large.

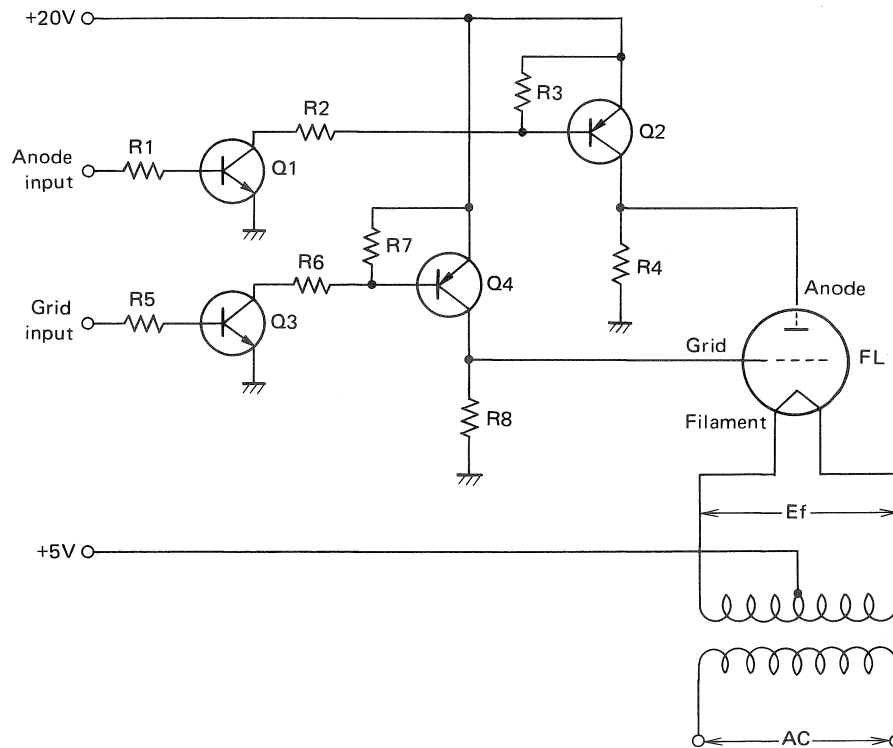


Fig. 23 Drive Circuit for FL

3. Liquid-crystal Display (LCD)

An LCD is not a luminous device like an LED or FL. An LCD allows injected light to pass, reflect, or be absorbed when a voltage is applied. LCDs can be roughly classified into two types: Dynamic Scattering Mode (DSM) type, and Field Effect Mode (FEM) type. Twisted Nematic (TN) type, a variety of FEM type, is the most popular. Let's discuss the TN LCD.

3.1 Structure and Features of LCD

Fig. 24 shows the basic structure of a TN LCD. The LCD has been made of layers of glass, transparent electrodes, and liquid crystal, like a sandwich. The molecules of the liquid crystal are piled up spirally as illustrated and turn the polarity of the injected light by 90 degrees.

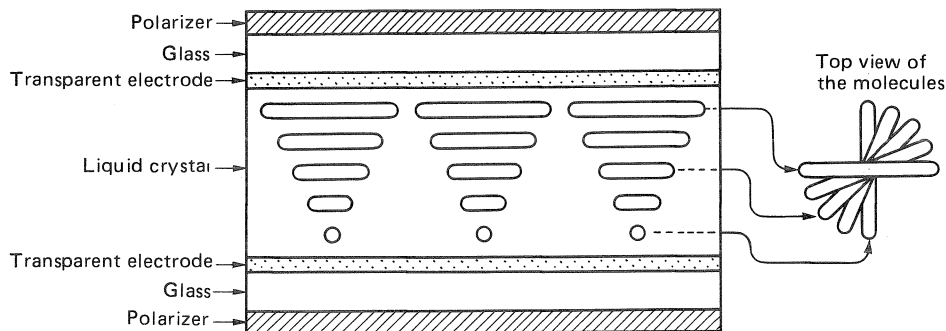


Fig. 24 Structure of TN LCD

a) Principles of operation

The structure and operational principles of an LCD are shown in Fig. 25

The thickness of the LCD is only a few millimeters, and that of the liquid-crystal layer is about 10 microns.

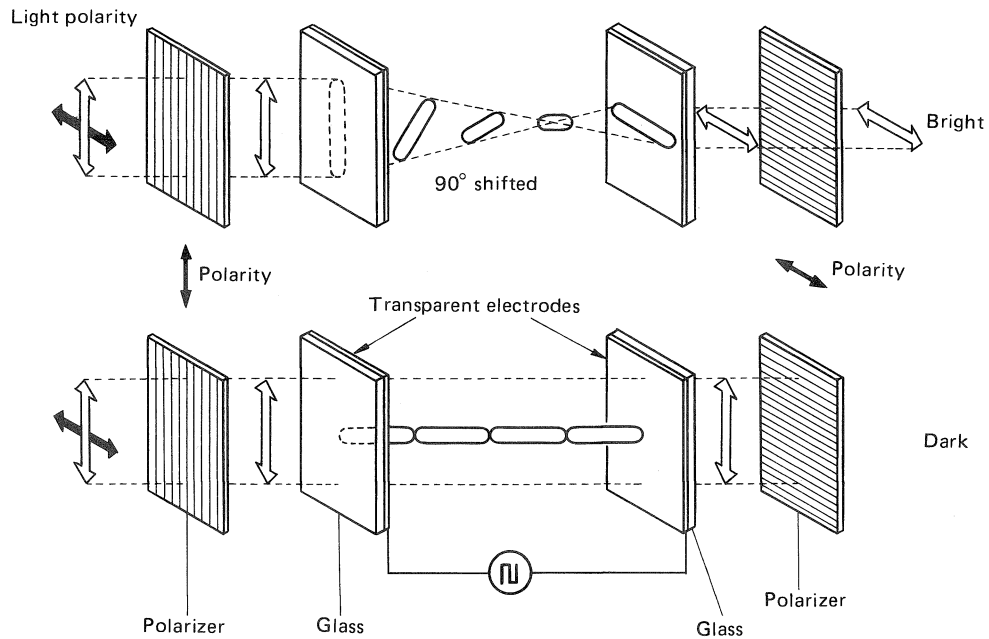


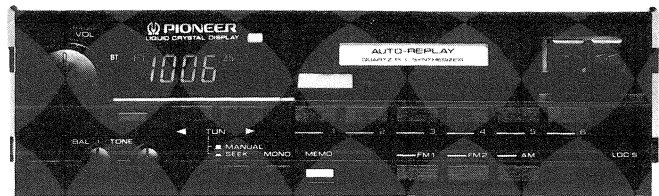
Fig. 25 Structure and Operational Principles of TN LCD

In Fig. 25, the first polarizer vertically polarizes the light coming from the left. When no voltage or electric field is applied to the transparent electrodes, the polarity of the light is turned by 90 degrees by the twisted crystal molecules and becomes horizontal; the second polarizer allows the horizontally polarized light to pass. When a voltage is applied between the electrodes, the crystal molecules are

aligned and let the light travel straight. The vertically polarized light is then intercepted by the second polarizer, which allows only horizontally polarized light to pass, and the intercepted areas on the screen become dark (Photo 5(a)). There is a type of inverse operation with parallel polarizers. This allows the rear light to pass and brighten the front screen when a voltage is applied (Photo 5(b)).



(a) KE-A630



(b) KE-4700

Photo 5 LCDs Employed in Car Stereos

b) Structure of LCD

Fig. 26 shows the structure of the LCD. A lamp is installed on both sides of a plate lens. The lamp light is scattered by the lens and by the diffusing plate to evenly illuminate the whole area of the LCD. Power is supplied from the circuit pattern to the LCD via conductive rubber in the rubber connector.

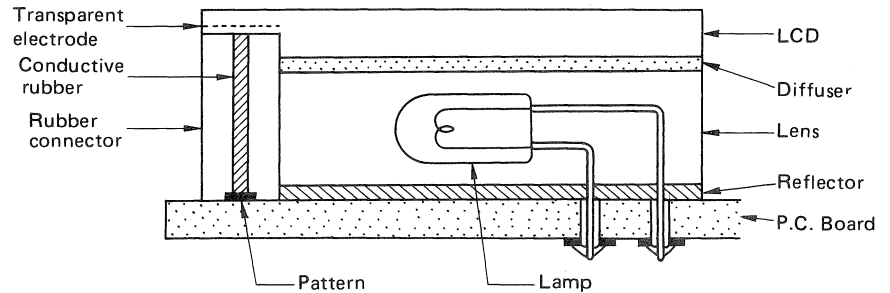


Fig. 26 Construction of LCD (Side view)

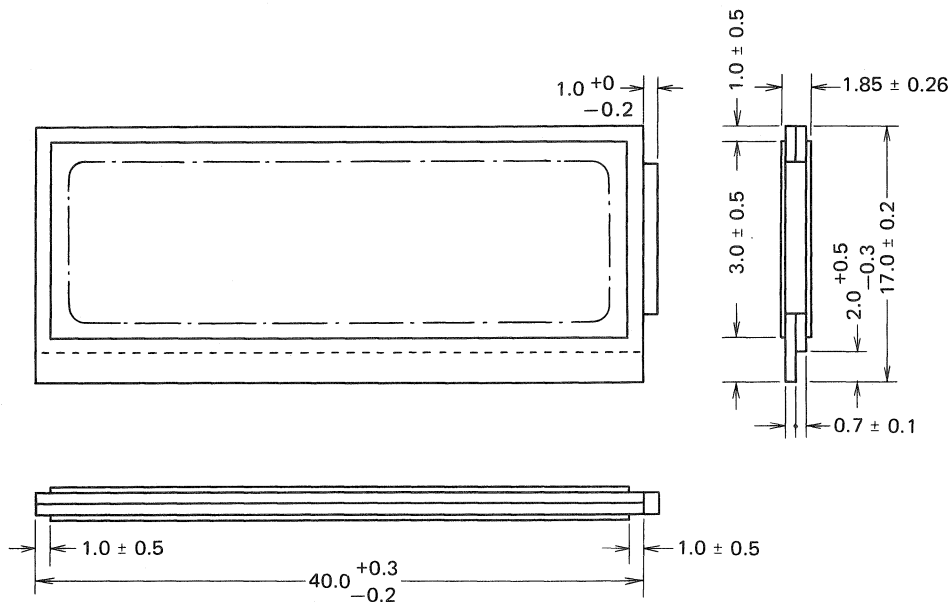


Fig. 27 LCD FTD-6081H

3.2 Characteristics of LCD

a) Characteristic of applied voltage vs contrast of LCD
 Contrast (relative value) represents the performance of an LCD because the LCD is not self-luminant. The voltage is indicated as zero-to-peak value $[V_{OP}]$ because a pulsed current is used (64 Hz square wave). If direct current is applied, the liquid crystal reacts, electrochemically, shortening the service life.

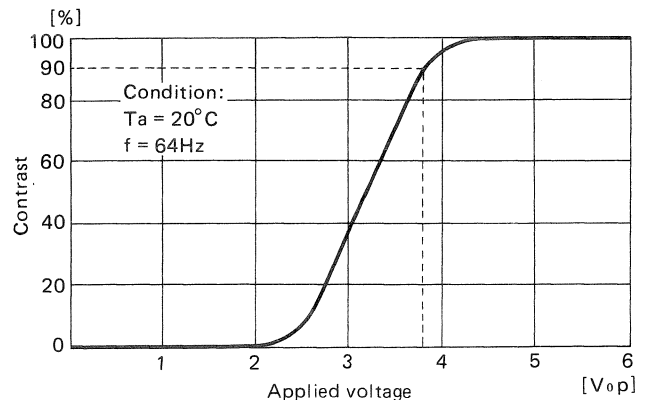


Fig. 28 Voltage vs. Contrast of LCD

b) Response speed of LCD

Fig. 29 shows the response speed of an LCD. Generally, the rise time (t_r) and fall time (t_d) of an LCD are from 30 to 100 ms each. (They are very slow compared with those of an LED or FL.)

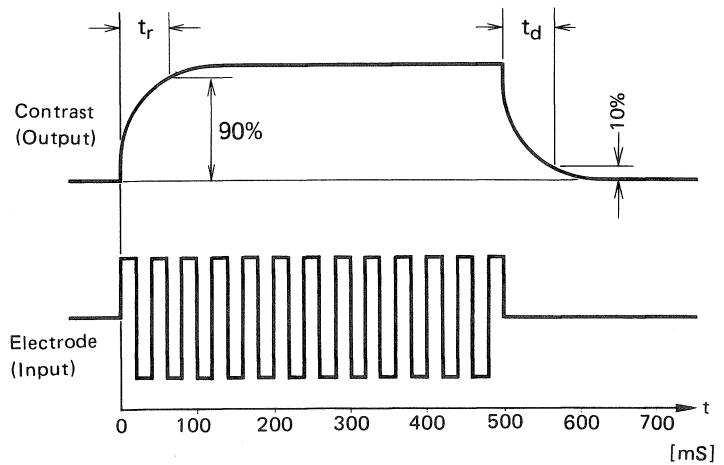


Fig. 29 Response Characteristic

3.3 Drive circuit

The working voltage of an LCD is usually set at 5 Vop to get the best contrast ratio and long service life. The frequency of the drive signal is from 30 to 100 Hz. The reasons for this are that signals at less than 30 Hz cause flickering, and signals at more than 200 Hz increase power consumption and prevent the slowly responding LCD from following the high-frequency signal. Power consumption of an LCD is very low, from several to tens of microamperes even when four-figure segments are driven (T_a : 25°C, f : 64 Hz, V : 5 V_{OP}). So the gate outputs of a MOS IC can drive an LCD without the help of any special drive IC.

a) Static drive

There are two drive methods: static and 1/2 duty-1/2 bias. Fig. 30 shows the connection of the four-character static drive system. The upper circuit has a common line and the lower has separate segment electrodes. A drive voltage is applied to both common and segment electrodes to illuminate a segment.

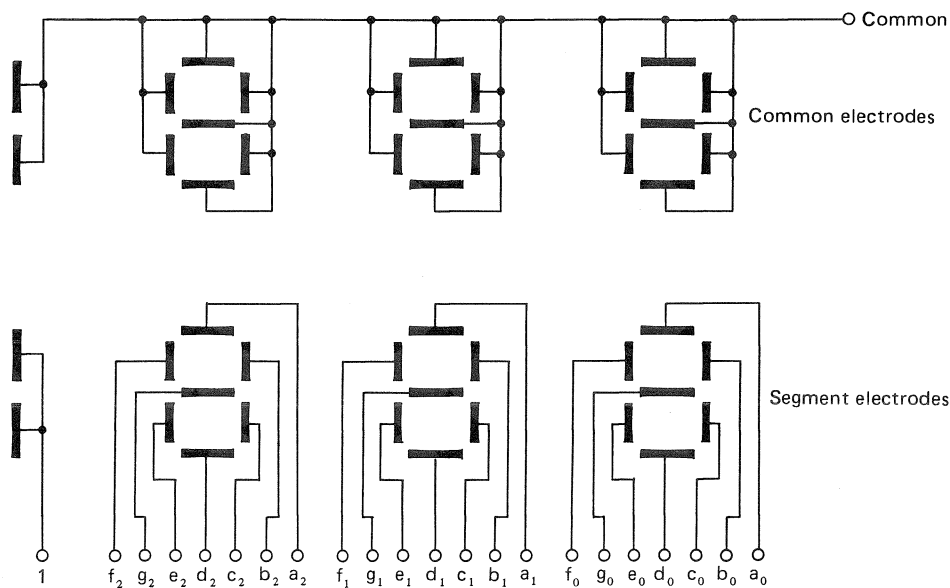


Fig. 30 Connection of Static Drive System

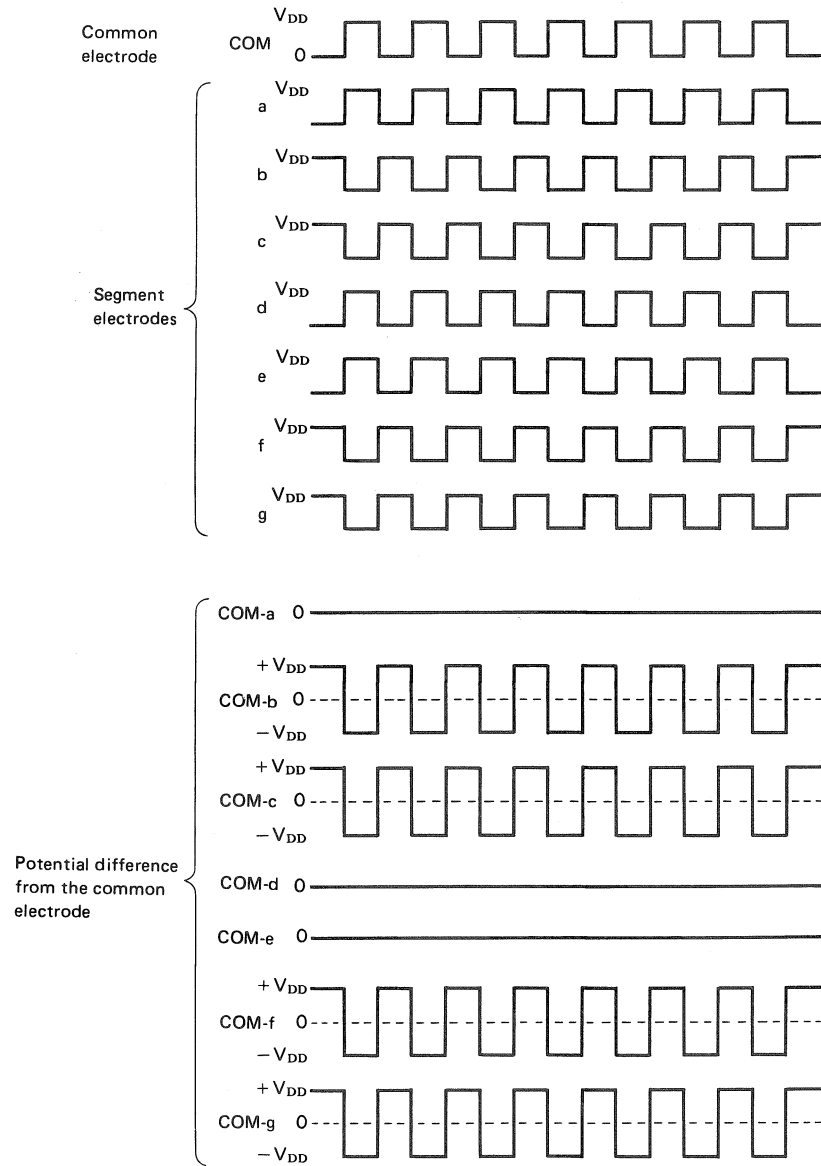


Fig. 31 Waveforms of the Drive Signals of the Static Drive System for Indicating the Figure 4.

Fig. 31 shows the waveforms of the drive signals when the LCD displays a 4. When the signals at the common and segment electrodes are in phase, no potential difference appears between the two electrodes. When they are 180 degrees out-of-phase and the potential at the common electrode is considered to be the reference voltage, 0 V , $+V_{DD}$ and $-V_{DD}$ alternately appear at the segment electrode. The LCD displays a figure 4 when the voltage to the segment electrodes (b, c, f, and g) is 180 degrees out of phase to that of the common electrode.

b) 1/2-duty 1/2-bias drive

Fig. 32 shows a 1/2-duty 1/2-bias drive circuit. The upper circuit has two common lines. The lower circuit has been simplified. Common-1 and common-2 select four and three segments respectively.

Fig. 33 shows the waveforms of the drive signals of the 1/2 drive system for indicating 4. The potential difference between the two electrodes is alternately $+V_{DD}$ and $-V_{DD}$ at the selected segments (b, c, f, and g), and is alternately $+V_{DD}/2$ and $-V_{DD}/2$ at the non-selected segments (a, d and e). The latter levels are not high enough to activate the segments. If the power supply circuit becomes defective, V_{DD} may become excessive, and all segments may be activated.

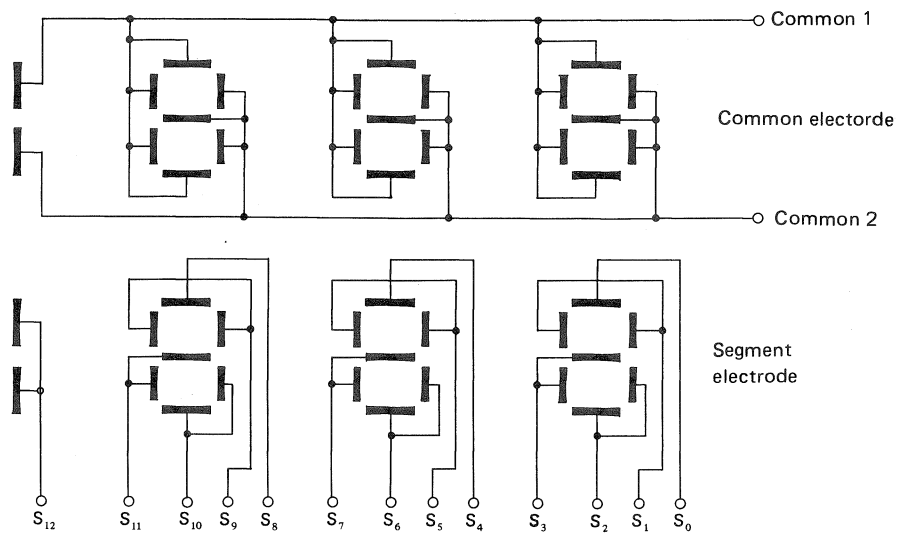


Fig. 32 Connection of 1/2-Duty 1/2-Bias Drive Circuit

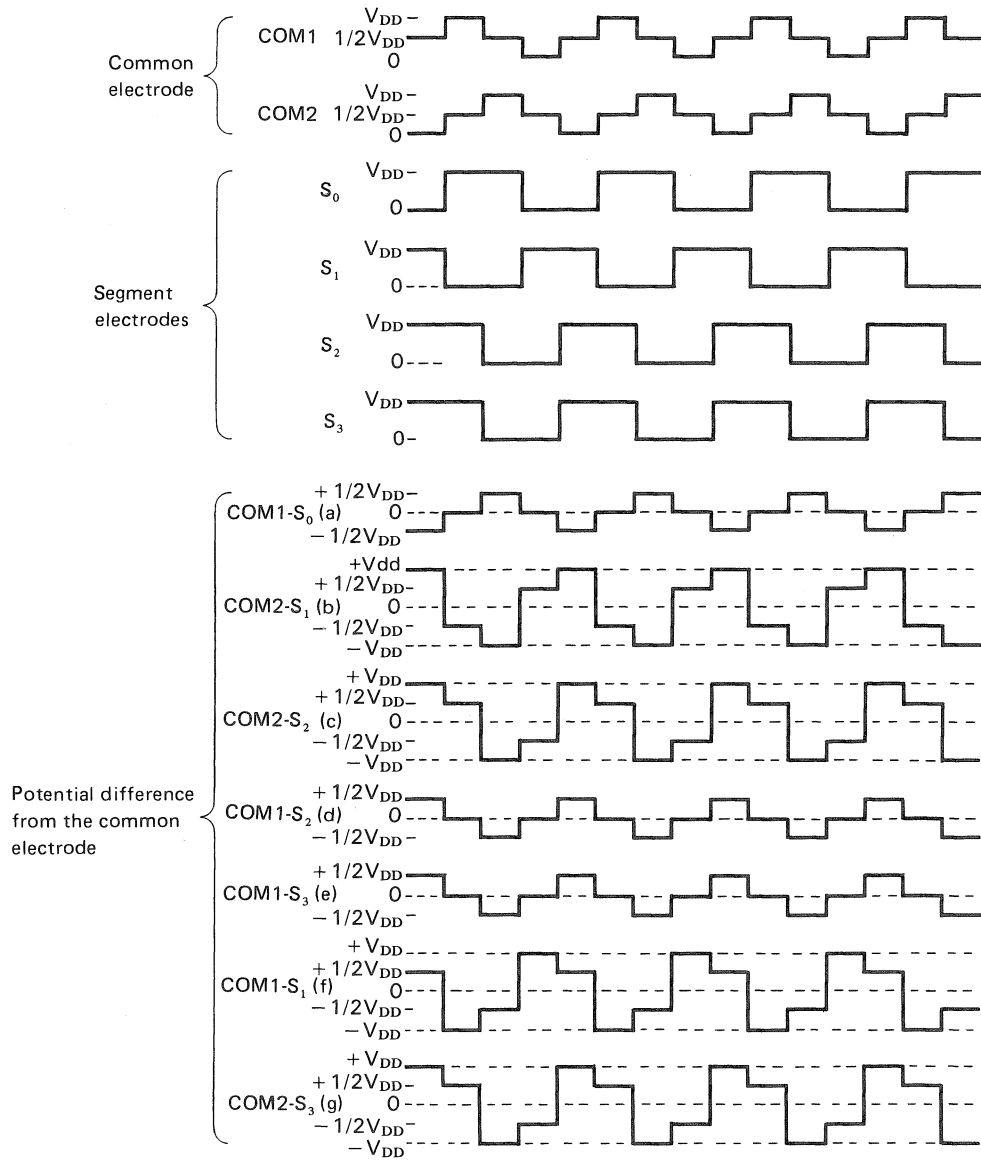


Fig. 33 Waveforms of the Drive Signals of the 1/2-Duty 1/2-Bias Drive System

Basic Theory of Electricity

OPERATIONAL AMPLIFIER (OP AMP)

1. What is an Op Amp

An op amp is a kind of differential amp that performs various mathematical operations. Application of negative feedback to a high-gain DC amp produces a circuit with a precise gain characteristic that depends on the feedback used. By selecting feedback components, operational amplifier circuits can be used to add, subtract, compare, integrate, and differentiate. The whole device has been integrated into one small IC and is widely employed in many types of equipment.

2. Differential Amplifier (Diff Amp)

A typical diff amp has three terminals: (+) and (-) inputs and an output. The (+) sign means that the signal applied to it is in phase to the output and does not mean a positive terminal. The (-) sign is inverted at the output and does not mean a negative terminal. The difference voltage between the input terminals is amplified and appears at the output terminal. The variation of like voltages or currents in phase each other at the inputs is suppressed and does not appear at the output. Fig. 1 shows a diff amp. When signals of 2V and 1V are applied to the (+) and (-) terminals of a 10 times amplifier, the output is 10V.

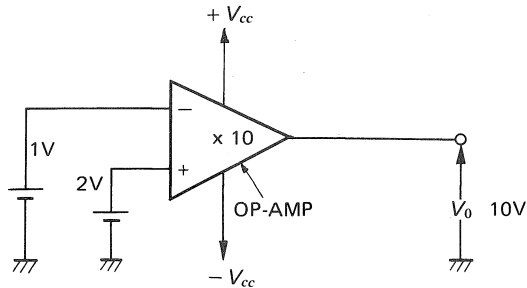


Fig. 1 Differential Amplifier

Hereafter, the power supply lines of the circuit (+ V_{cc} and $-V_{cc}$) will be omitted from the figures.

3. Ideal Op Amp

It is easy to understand op amps by imagining an ideal op amp having the following characteristics:

Amplification is infinite.

Input impedance is infinite.

Output impedance is null.

Wide frequency response (0 Hz to several MHz)

Current/voltage offset is null.

No current flows internally between the two input terminals. When no signals are applied to the inputs, the voltage difference between the input terminals is null. The input terminals are viewed as shorted (imaginary short) for voltage and open for current when NFB is applied.

4. Basic Circuits

Inverting Amp

Fig. 2 shows an inverting amp. By grounding the (+) terminal and applying v_1 (input signal) to the (-) terminal, we can obtain an inverted and amplified signal, v_o , at the output. Let's look at the relationship between v_1 and v_o . Assume that voltage difference between the (+) and (-) terminals is v_s . If 1V is applied to (a), the voltage v_{R1} across R_1 and the current i_1 through R_1 become:

$$v_{R1} = 1 \text{ [V]} - v_s$$

$$i_1 = \frac{1 \text{ [V]} - v_s \text{ [V]}}{10 \text{ [k}\Omega\text{]}}$$

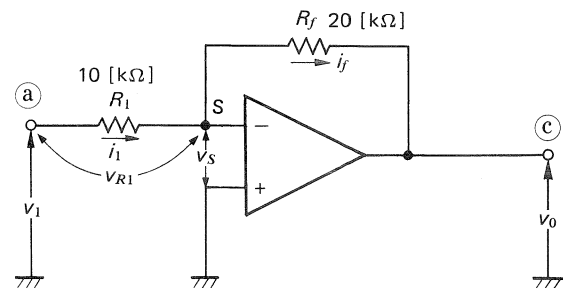


Fig. 2 Inverting Amplifier

Here, no current flows into the (-) terminal because the input impedance is infinite. i_1 then, flows to \textcircled{c} .

$$i_f = \frac{v_S [V] - v_0 [V]}{20 [k\Omega]}, \quad i_1 = i_f$$

$$\frac{1 [V] - v_S [V]}{10 [k\Omega]} = \frac{v_S - v_0}{20 [k\Omega]} \dots \dots \dots (1)$$

If the amplitude is A.

$$v_0 = A v_S, \quad v_S = \frac{v_0}{A}$$

v_S becomes 0 because A is infinite.

This phenomenon is “imaginary grounded” because it appears as if the input terminal were grounded for voltage. Because the input impedance is infinite, the impedance can be changed by adding an input resistor between the input terminal and ground.

When 0 is substituted for v_S in the formula (1)

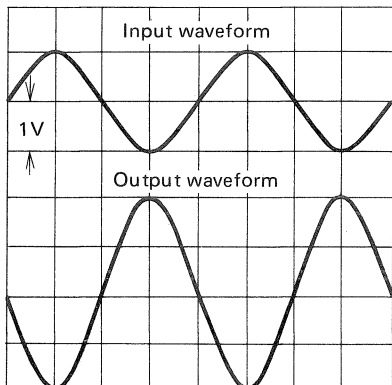


Fig. 3 Input/Output waveforms of

$$\frac{1 [V]}{10 [k\Omega]} = \frac{-v_0}{20 [k\Omega]}$$

$$\therefore v_0 = \frac{-20 [k\Omega]}{10 [k\Omega]} \times 1 [V] = -2 [V]$$

So, v_1 is inverted and amplified by two, then appears at the output. The gain of the amplifier is determined by the resistance ratio of R_f/R_i . The gain then becomes 2. Fig. 3 shows the waveforms of sine input applied to the op amp and the resulting output signal.

In Fig. 2, the moment when v_1 is applied to \textcircled{a} , a voltage lower than v_S appears at the (-) terminal (S). v_S appears, although it is very small because both input terminals are imaginary shorted. v_d is amplified. A large voltage appears at the output because the gain of the op amp is infinite. Much of the output voltage however, is negatively fed back to (S) via R_f to cancel the input signal and to balance the circuit. v_S decreases. The output decreases. Feedback voltage decreases. v_S increases again. This circular operation is performed repeatedly until the output voltage stabilizes at a certain point.

In Fig. 4, DC bias currents I_{B1} and I_{B2} usually flow even when no signal is applied.

Temperature effects the bias currents and output. To prevent the currents from flowing and to make an ideal op amp we insert a compensating resistor, R_c , between the (+) input and ground, as shown in Fig. 5. Here,

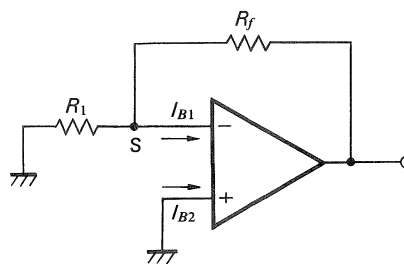


Fig. 4 Offset Voltage

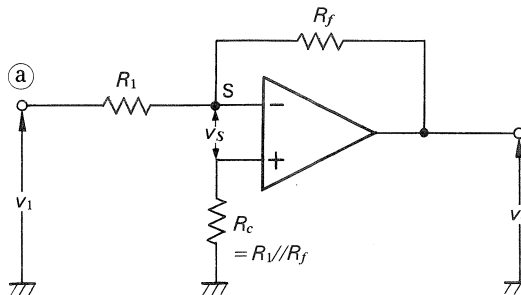


Fig. 5 Offset Canceller

Noninverting Amp

A diff amp having its output in phase with the input is called a noninverting amp. Fig. 6 shows a noninverting amp. In this case, the input signal is applied to the (+) terminal. The relationship between v_1 and v_o is as follows: $v_s = 0$ due to imaginary short. The voltage at the (-) terminal becomes equal to v_1 . No current flows in or out of the (-) terminal because the input impedance is infinite. Thus i_i becomes equal to i_f .

$$i_i = \frac{v_1 \text{ [V]}}{10 \text{ [k}\Omega]} \quad (v_s = 0)$$

$$i_f = \frac{v_o \text{ [V]} - v_1 \text{ [V]}}{10 \text{ [k}\Omega]}$$

$$i_f = i_i$$

$$\therefore \frac{v_1 \text{ [V]}}{10 \text{ [k}\Omega]} = \frac{v_o \text{ [V]} - v_1 \text{ [V]}}{10 \text{ [k}\Omega]} \dots \dots \dots (2)$$

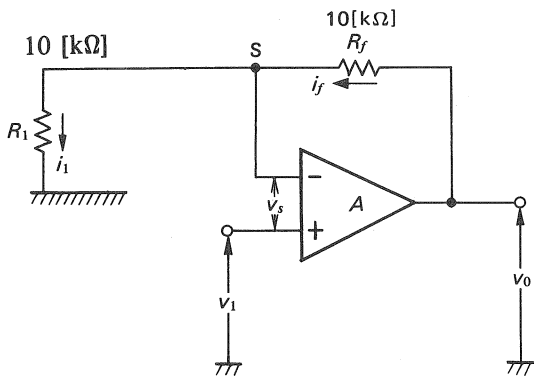


Fig. 6 Noninverting Amp

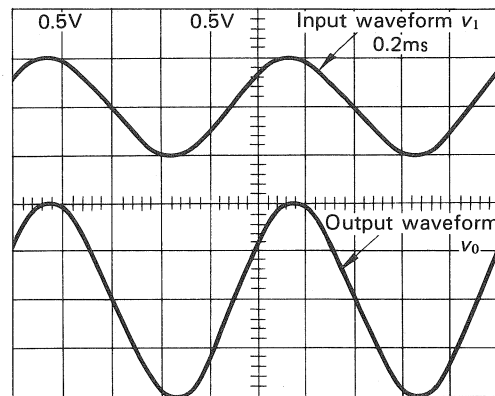
$$10 \text{ [k}\Omega] \times v_1 = 10 \text{ [k}\Omega] (v_o \text{ [V]} - v_1 \text{ [V]})$$

$$\therefore (10 \text{ [k}\Omega] + 10 \text{ [k}\Omega]) v_1 \text{ [V]} = 10 \text{ [k}\Omega] \times v_o$$

$$\therefore v_o \text{ [V]} = \left(1 + \frac{10 \text{ [k}\Omega]}{10 \text{ [k}\Omega]}\right) v_1$$

$$G = \frac{v_o \text{ [V]}}{v_1 \text{ [V]}} = 1 + \frac{10 \text{ [k}\Omega]}{10 \text{ [k}\Omega]} = 2$$

In Fig. 6, the moment a signal is applied to the (+), v_s appears, although it is very small. It is amplified and appears at the output. Much of v_o is negatively fed back to (S) via R_f (10KΩ) to minimize v_s . v_s decreases. v_o decreases. Feedback decreases. v_s increases. v_o increases again. This circular operation repeats quickly until the circuit balances and stabilizes at a certain point. The gain of this amp is the ratio of v_o/v_1 . Fig. 7 shows the input and output signal when $G=2$.



$f = 1\text{kHz}$ Closed loop gain $G = 2$

Fig. 7 Input/Output Waveform of a Noninverting Amp

a) Inverting adder

This is an adder made of an inverting amplifier. The relationship among v_1 , v_2 , and v_o is as follows: Pin S is imaginary grounded because the (+) and (-) inputs are imaginary shorted and the (+) input is grounded. So the following formulas apply:

$$i_1 + i_2 = i_f$$

because the input impedance of op amp is infinite.

$$i_1 = \frac{v_1 - v_S}{R_1}, \quad i_2 = \frac{v_2 - v_S}{R_2}$$

$$i_f = \frac{v_S - v_0}{R_f}$$

$$\therefore \frac{v_1 - v_S}{R_1} + \frac{v_2 - v_S}{R_2} = \frac{v_S - v_0}{R_f} \dots \dots \dots (3)$$

When 0 is substituted for v_S ,

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} = - \frac{v_0}{R_f} \dots \dots \dots (4)$$

Here,

$$R_1 = R_2 = R_f$$

$$v_0 = - (v_1 + v_2)$$

Thus the resulting sum is inverted and appears at the output terminal. Fig. 8 shows that v_1 and v_2 are added and the resulting signal is inverted.

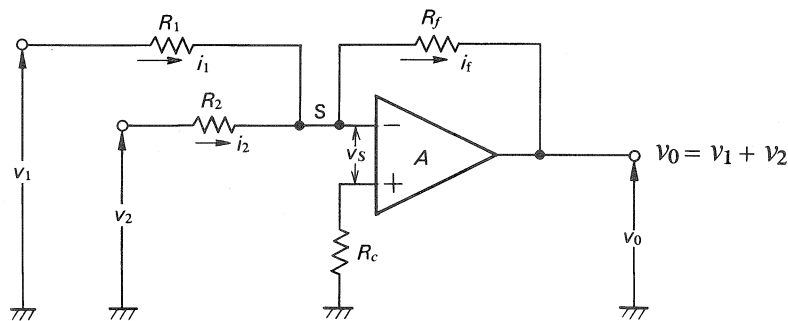


Fig. 8 Adder

b) Differential input subtractor

In Fig. 9, two resistors of equal value R_1 and R_2 are connected symmetrically to the (+) and (-) terminals. If the voltages at (n) and (p) are v_n and v_p respectively, the formulas shown below are obtained:

$$i_1 = i_{f1}, \quad i_2 = i_{f2}$$

$$v_p = R_C \times i_{f2}$$

$$i_{f2} = \frac{v_2}{R_2 + R_C}$$

because no current flows into the (+) terminal.

$$v_p = \frac{R_C}{R_2 + R_C} v_2 \dots \dots \dots (5)$$

$$i_1 = \frac{v_1 - v_n}{R_1}, \quad i_{f1} = \frac{v_n - v_0}{R_f}$$

$$i_1 = i_{f1}$$

$$\therefore \frac{v_1 - v_n}{R_1} = \frac{v_n - v_0}{R_f} \dots \dots \dots (6)$$

$v_n = v_p$ because n and p are imaginary shorted. When the formula (5) is substituted into the formula (6),

$$\frac{v_1 - \frac{R_C}{R_2 + R_C} v_2}{R_1} = \frac{\frac{R_C}{R_2 + R_C} v_2 - v_0}{R_f} \dots \dots (7)$$

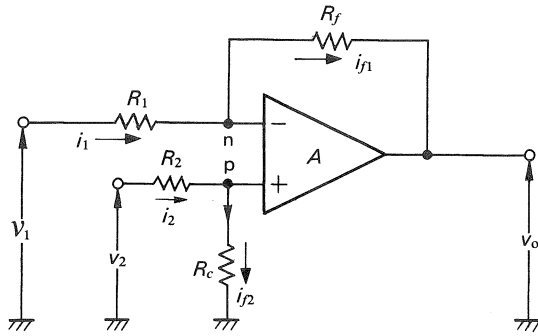


Fig. 9 Input Subtractor

From (7)

$$v_0 = \frac{R_c(R_1 + R_f)}{R_1(R_2 + R_c)} V_2 - \frac{R_f}{R_1} V_1 \quad \dots \dots (8)$$

When $R_1 = R_2 = R_f = R_c$, the circuit operates as a subtractor and gives.

$$v_0 = V_2 - V_1$$

The function can be checked by applying the same signal to both inputs. The output will be 0V.

Fig. 11 shows an example of the circuit employed in the focusing and tracking systems of the LD-700 for detecting errors.

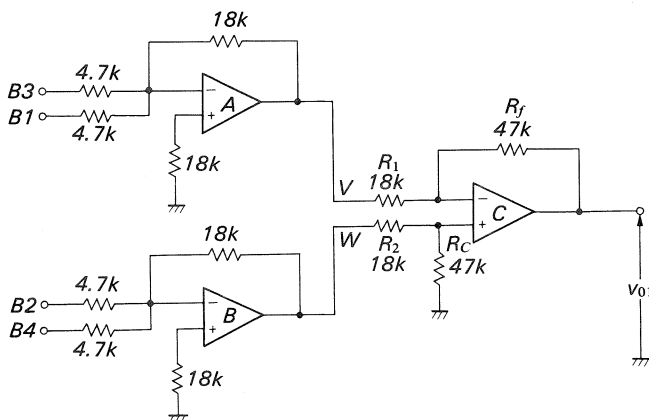


Fig. 11a Focus Servo Circuit of LD-700

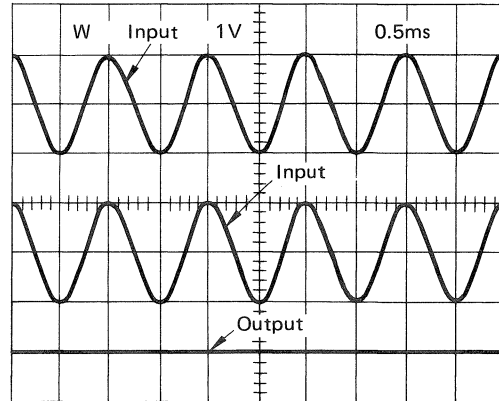


Fig. 10 Input/Output waveforms of Differential Input

Fig. 11a shows a simplified focusing servo circuit. The relation between inputs (B1 — B4) and outputs (V and W) is as follows: Amp A is an adder. When the values of resistors are substituted for the variables of the formula (4).

$$v_V = -\frac{18 \text{ [k}\Omega]}{4.7 \text{ [k}\Omega]} (B_1 + B_3)$$

Amp B is also an adder, so

$$v_W = \frac{18 \text{ [k}\Omega]}{4.7 \text{ [k}\Omega]} (B_2 + B_4)$$

Next, let's look at the relationship of V and W to v_{o1} . Because the circuit is a subtractor, the above values can be substituted into the formula for a subtractor (8):

$$R_c = R_f = 47 \text{ [k}\Omega]$$

$$R_1 = R_2 = 18 \text{ [k}\Omega]$$

$$\therefore v_{o1} = \frac{47(18 + 47)}{18(18 + 47)} W - \frac{47}{18} V$$

$$= \frac{47 \text{ [k}\Omega]}{18 \text{ [k}\Omega]} (W - V)$$

$$\therefore v_{o1} = \frac{47}{18} \times \frac{18}{4.7} \{ (B_1 + B_3) - (B_2 + B_4) \}$$

$$= 10 \{ (B_1 + B_3) - (B_2 + B_4) \}$$

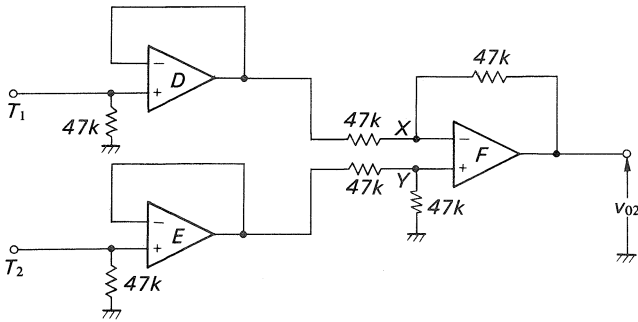


Fig. 11b Tracking Circuit of LD-700

Fig. 11b shows a portion of the tracking servo circuit, LD-700. The relationship between the inputs (T1 and T2) and the outputs (X and Y) is as follows. Circuits D and E are noninverting amps. The inputs appear directly at the outputs. Circuit F is a subtractor. Because the values of all resistors are equal,

$$\begin{aligned}
 V_{02} &= Y - X \\
 &= T_2 - T_1
 \end{aligned}$$

Comparator

So far, we have discussed op amps with a negative feedback (NF) loop. What will happen when the NF loop is open. Fig. 12 shows the basic circuit of a comparator.

A reference level (v_{ref}) is applied to either of the input terminals and the voltage to be compared, v_i , is applied to the other terminal. The input signal level (or phase) is compared with the reference voltage. In Fig. 12, a reference voltage is applied to the (+) terminal, and the signal to be compared is applied to the (-) terminal. If the gain of the amplifier is 10^6 , v_{ref} is 2V and v_i is 2.01V.

$$v_0 = A(v_{ref} - v_i) = 10^6 (2 - 2.01) = -1000 \text{ [V]}$$

Actually, the voltage saturates before it reaches the bias level. The lowest level becomes $-V_{cc} + 1V$ to $-V_{cc} + 2V$, not $-V_{cc}$, because of the internal suction voltage of the op amp. If $-V_{cc}$ is $-12V$, $-E_{os}$ is nearly $-10V$. If v_i is 0.01V lower than the v_{ref} , the output is $+E_{os}$ 10V. See Fig. 13.

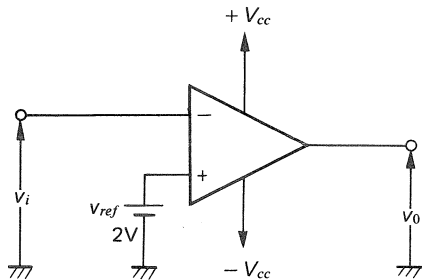


Fig. 12 Comparator

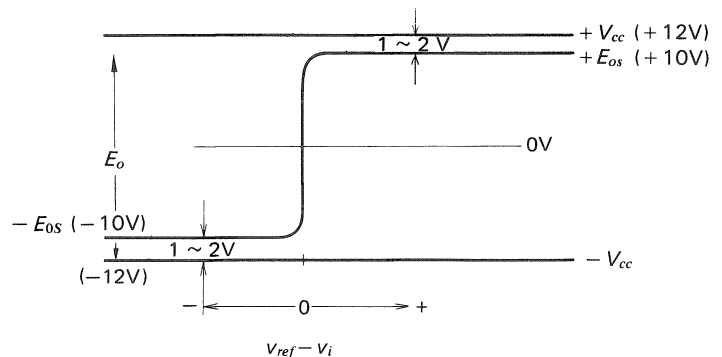


Fig. 13 Input vs. Output of a Comparator

First Step in Audio and Video

Specifications

TV Resolution

The resolution of a television receiver is expressed by the maximum number of lines discernible on the screen at a distance equal to cathode-ray tube (CRT) height. This is the most important among TV specifications. When a pattern of black and white stripes is displayed on the screen and the pitch of the stripes is gradually minimized, the black and white lines become undiscernible. A system having high resolution can display fine, clear pictures.

There are two kinds of resolution: horizontal resolution, and vertical resolution. Horizontal resolution is usually discussed because vertical resolution is determined by the number of scanning lines specified by the TV broadcast system. The horizontal resolution is determined by the video frequency characteristic shown in Fig. 1. Broadcasting frequency range allocated for one channel has been limited by TV format. A picture is reproduced on the screen by scanning an electron beam horizontally and vertically. In the NTSC (National TV Standards Committee) system, the horizontal scanning period is $52.7\mu\text{s}$. Fig. 2.

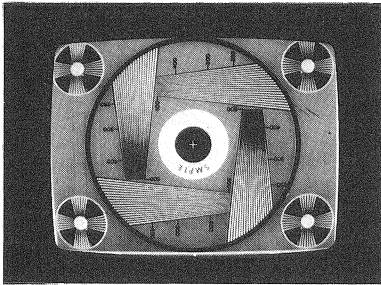


Photo 1 Test Pattern

When the video frequency is f MHz, the number of signal waves displayed on one scanning line is $f \times 52.7$. The number of picture elements is twice the number of waves ($f \times 52.7 \times 2$) because a pair of black and white dots, or low and high levels, represents one wave. The number of horizontal and vertical picture elements or stripes are counted in a square area with the sides equal to the height of the screen. Three-fourths of the horizontal elements are then taken, because the aspect ratio of the screen size is 3 to 4. The relationship between the video frequency bandwidth and resolution is as follows:

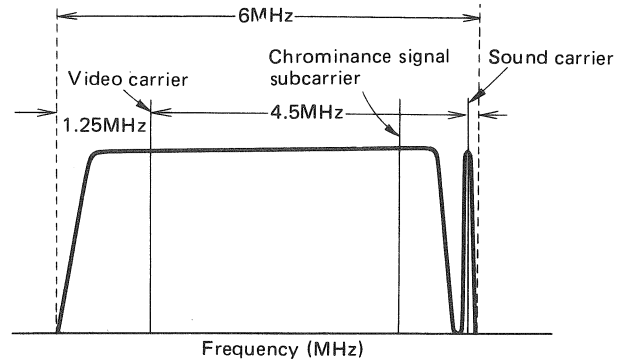


Fig. 1 Frequency Spectrum of Television Waves (NTSC)

f : Video frequency bandwidth [MHz]

N : Horizontal resolution (number of lines)

$$N = 3/4 \times 106 \times f$$

The broader the video frequency bandwidth, the higher the horizontal resolution. The frequency bandwidth of video signals extends to the point of -20 dB response far below -3 dB (-3 dB is popularly used in audio systems), because human eyes can discern high-frequency video signals of -20 dB response. If a TV set has horizontal resolution of 400 lines, it can reproduce video signals at 5 MHz.

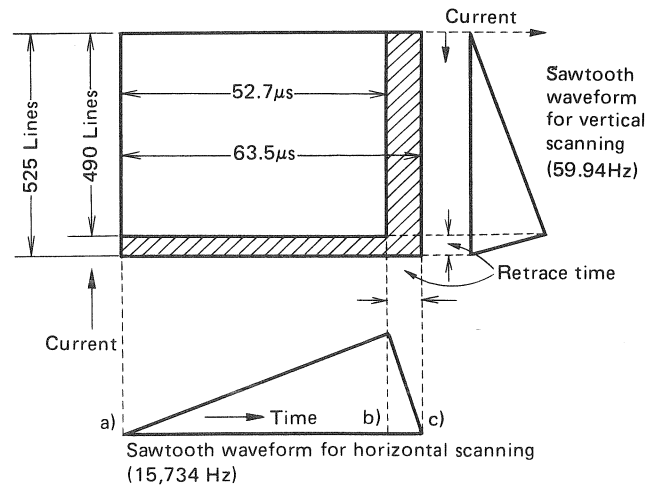


Fig. 2 Sawtooth Waveform (NTSC)

In other words, the 5 MHz frequency range is required to reproduce 400 vertical lines. The NTSC video signal now being broadcast is within 4.3 MHz which provides 350 lines. Having a resolution of 400 lines, PIONEER TV monitors such as the SD-25 have an ability to reproduce finer pictures than those being broadcast. In measuring the resolution, use a test pattern that has a greater frequency bandwidth than that actually being broadcast. The numbers shown along the lines of the test pattern on the screen indicate the discernible limit of the lines. The LD system requires a high-quality TV monitor because discs have a resolution of 350 lines. In the PAL (Phase Alternation Line) system, the number of scanning lines is 625, so its vertical resolution is higher than that of the NTSC system. Its number of frames per second (25 fs), however, is less than that of NTSC (30 fs), so its pictures flicker.

As mentioned above, the resolution of a TV system depends on the frequency bandwidth of broadcast video signals and the number of scanning lines, whereas the resolution of camera film depends on lenses and the dimensions of silver nitrate particles on the film.

Resolution of various systems

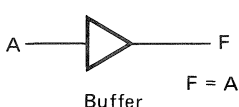
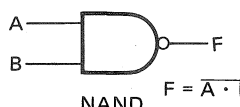
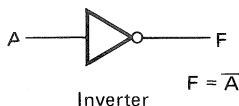
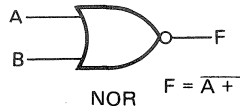
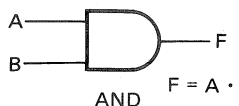
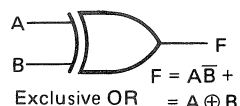
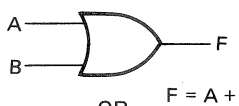
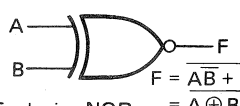
Conventional TV receives	(NTSC)	about 250 lines
VCR	(NTSC)	about 250 lines
LD	(NTSC)	about 350 lines
Personal computer display		about 640 lines (or 4,050 characters)

One Point Servicing Techniques

Troubleshooting Digital Circuit

1. Logic Circuits in Digital ICs

A logic circuit switches "ON" and "OFF" and puts out only a high (H) or low (L) signal. It has no in-between levels.

Logic input	Function table	Logic input	Function table																														
 <p>Buffer $F = A$</p>	<table border="1"> <thead> <tr> <th>A</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	F	L	L	H	H	 <p>NAND $F = \overline{A \cdot B}$</p>	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> </tr> </tbody> </table>	A	B	F	L	L	H	L	H	H	H	L	H	H	H	L									
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A	B	F																															
L	L	H																															
L	H	L																															
H	L	L																															
H	H	H																															

H: High level
L: Low level

Fig. 1 Logic Circuits and Truth Tables

A knowledge of the functions of basic logic circuits shown in the truth tables in Fig. 1 is sufficient for understanding this chapter. Refer to "DIGITAL, Supplement to TUNING FORK" for details. Every digital circuit consists of logic circuits. But there is no description of IC logic circuits on circuit diagrams. It is easy to understand and diagnose the problems of a circuit that has just a few logic circuits, but not a circuit that has many logic circuits.

A digital circuit has "INPUT(S)" to receive information, "OUTPUT(S)" to pass the processed results to following stages and "POWER line(s)". An IC also has the same terminals. Measuring the input and output of an IC without considering the internal circuitry is usually enough, so most IC descriptions in service manuals are only pin numbers, functions and initial states. Troubleshooting can be done with a knowledge of the relation between the input and output. The problem is that input conditions differ according to the IC.

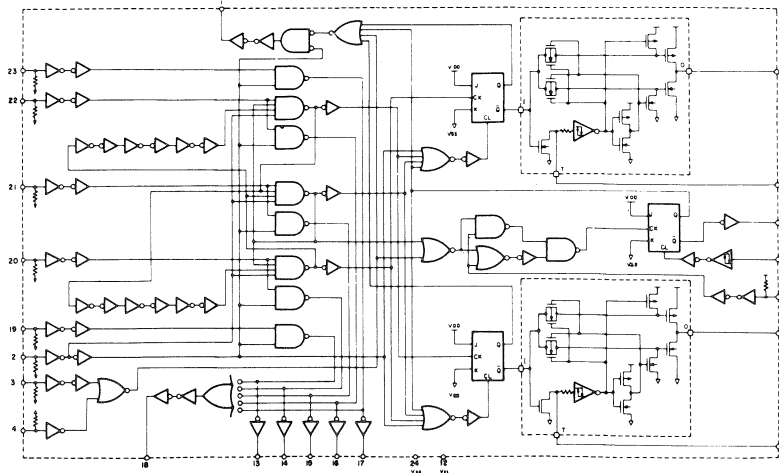


Table 1 Schematic Diagram of an IC

Pin No.	Pin Name	I/O	Function and Operation
1	MI	OUT	Muting output to prevent motor noise during FF/REW.
2	S	IN	Switches the tuner function and tape function of sets with an electronic tuner. Used at "H" for tuner and "L" (or open) for tape deck.
3	P	IN	Stop play direction switched by pin (2) (x3) during FF/REW. P or P̄ is used depending on the motor used in the deck.
4	P̄	IN	(1) When P is used, the direction change function is stopped by making P̄ open or "H" and P "L" or open. (2) When P̄ is used, the direction change function is stopped by making P open or "L" and P̄ "H" or open.
5	DR	IN	Switches the play running direction by means of the tape end sensing input. Has priority over all pin modes.
6	OP	OUT	Direction drive output. Output pin to drive the main solenoid. Pulse width is determined by the external circuit of pin (9)
7	OF	OUT	FF/REW drive output. Output pin which drives the sub solenoid. (3-STATE OUTPUT)
8	OR	OUT	 Pulse width is determined by the external circuit of pins (10) and (11)
9	T1		Sets the direction pulse width. Determines the output pulse width of pin (6) Pulse width $tw \approx 0.69CR$ (s) IC internal equivalent circuit

Pin No.	Pin Name	I/O	Function and Operation
10	T2		FF/REW output pulse width setting. Pulse width $tw \approx 0.69CR$ (s)
11	T3		
12	Vss		GND
13	V5		
17	Y1	OUT	Not used by KP-707G
18	M2	OUT	Not used by KP-707G.
19	X5	IN	GND
20	X4		Tape deck control input. Pin (20) → REW, Pin (23) → Direction, Pin (22) → FF
22	X2		
23	X1		GND
24	VDD		+B

Table 2 Function and Pin Alignment

2. High, Low and Threshold Levels

The necessary information for digital ICs is H or L level (voltage) only, in other words the ICs will not accept intermediate values. The border line between the H and L input levels is called the "threshold level" for logic circuits. This can be a problem, because there is a transition range where the IC cannot judge the level. See Fig. 2. The output becomes unstable when the input signal is close to the threshold level. The underterminable transition range depends on the type and peripheral components of the IC. The output may also be affected by external noise interference and supply voltage. Improper output of a stage will cause malfunctions at the following stages.

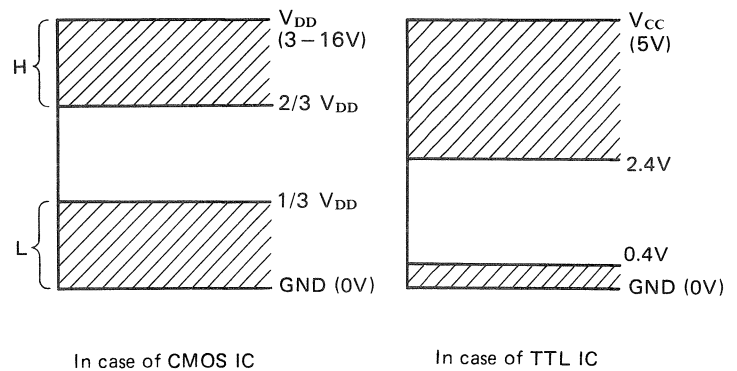


Fig. 2 High and Low Ranges

The H and L ranges of the logic level of the TTL (Transistor-Transistor Logic) IC and the CMOS (Complementary Metal-Oxide-Semiconductor) IC are different because their supply voltage and construction are different. The supply voltage for CMOS ICs is 3V to 16V and 5V for TTL ICs. H or L output is obtainable as long as the voltage fluctuation of the input signal is out of the threshold range. The circuits should have no intermediate level. If an intermediate level appears, there must be a faulty circuit upstream from the measured point. An IC with an intermediate output level must be faulty.

3. Input/Output Terminals and their Functions

There are two types of input terminals: a “high activity” type which requires an H signal to operate, and a “low activity” type which requires an L signal. To distinguish these in schematic diagrams, “low activity” types have a bar placed over them and “high activity” types have no bar. For example, “CS” and “RES”. The “high activity” type only becomes active when an H signal is applied to its input, and the “low activity” type when an L signal is applied. These discrete state also apply to outputs. So, when checking ICs, measure both input and output levels at active and inactive times referring to service manuals. It should be noted that there may either be just one narrow pulse or many repeating pulses.

3-1 Open Collector Output (TTL IC) and Open Drain Output (MOS IC)

The output terminal of open collector type TTL ICs is directly connected to the collector of the output transistor inside the IC.

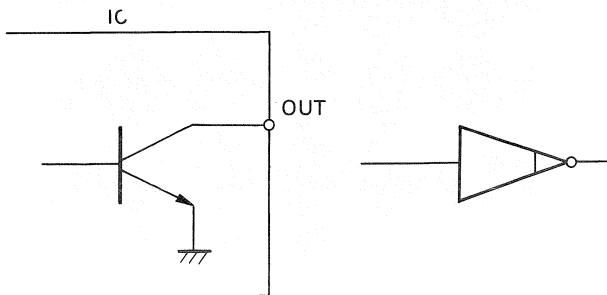


Fig. 3 Open Collector Output Symbol
(NOT circuit symbol)

In Fig. 3, the transistor turns on and V_{out} becomes L when V_b becomes 0.6V. It turns off and no voltage appears at the output when V_b becomes lower than 0.6V because the terminal opens. Although the meter now indicates 0V, it is not actually 0V. The output is just floating in “high impedance”. A regular type of logic circuit can be made with this IC and a pull-up resistor by supplying it with power via a pull-up resistor as shown in Fig. 4.

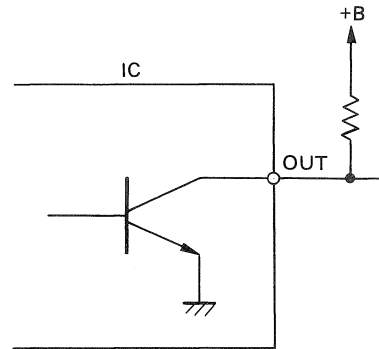


Fig. 4 Pull-up Resistor for an Open Collector IC

The output becomes L when V_b becomes 0.6V, and H when it is lower than 0.6V because the pull-up resistor supplies +B to the output terminal. The V_{out} can be adjusted by changing the resistor. With the help of the resistor, two circuits which are working on different levels such as TTL IC and MOS IC can be connected to each other. When checking the open collector IC, see if the output level shifts with the input level. If the level remains at L, open the output terminal and see if the input voltage of the following stage is H. If it is L, the following stage is faulty. There is an open drain output type of MOS IC, similar of the open collector type. It operates much like the open type.

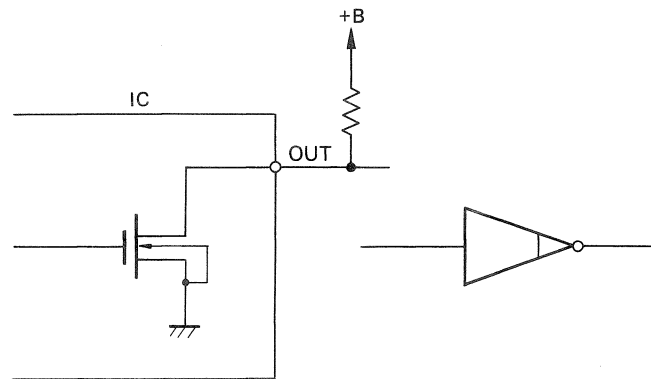


Fig. 5 Symbol of Open Drain Output Type IC

3-2 Power Supply

Power is required to operate an IC. There are positive and negative power sources. The power line terminals are named depending on the IC. See if the levels are equal to those shown on the circuit diagram.

IC	+	-
TTL	V_{CC}	GND
P-MOS	V_{SS}	V_{DD}
P-MOS	GND	V_{DD}
N-MOS	V_{DD}	V_{SS}
C-MOS	V_{DD}	GND
C-MOS	V_{DD}	V_{SS}

Fig. 6 Name of Power Supply

3-2 Clock

Generally, a microcomputer processes various functions with the timing given by periodic pulses called "clock pulses." The clock can be understood as a kind of power supply. After checking the power supply voltage, see if the clock pulses appear at the CLOCK input. Examples of the clock pulse oscillator and its output waveforms are shown below.

a) Crystal oscillator (Ceramic oscillator)

Crystal oscillators are employed in equipment which requires precise reference frequencies such as PLL synthesizers, system clocks and frequency dividers. The precision is dependent on the quality of the resonance material.

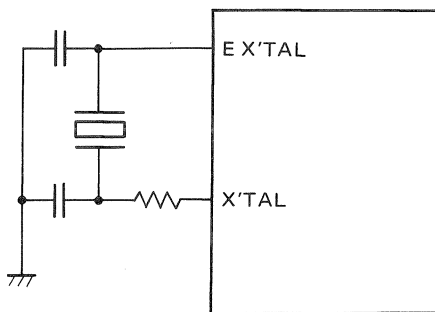


Fig. 7 X'tal Oscillator

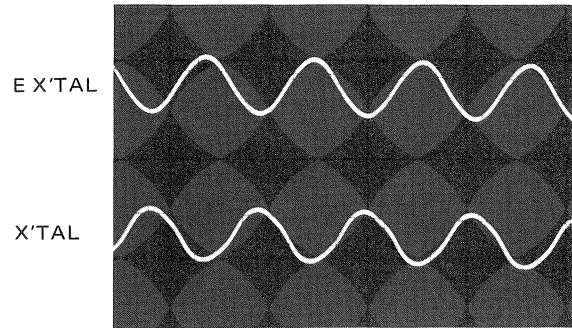


Photo 1 Waveform

b) RC oscillator

The frequency is determined by the time constant made by resistor(s) and capacitor(s). This is the most common types of oscillator.

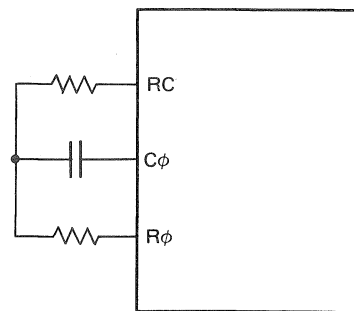


Fig. 8 RC Oscillator

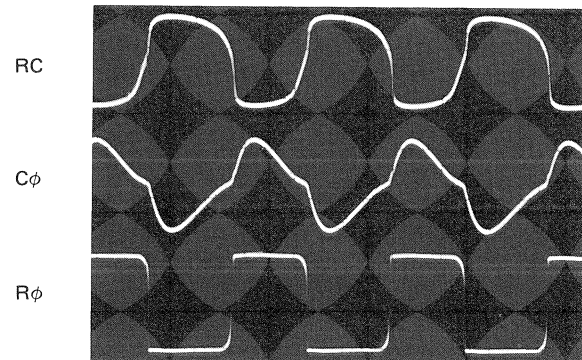


Photo 2 Waveform

c) LC oscillator

The frequency is determined by the time constant made by coil(s) and capacitor(s).

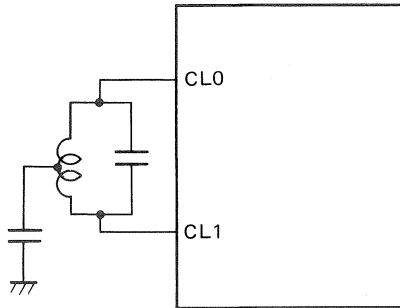


Fig. 9 LC Oscillator

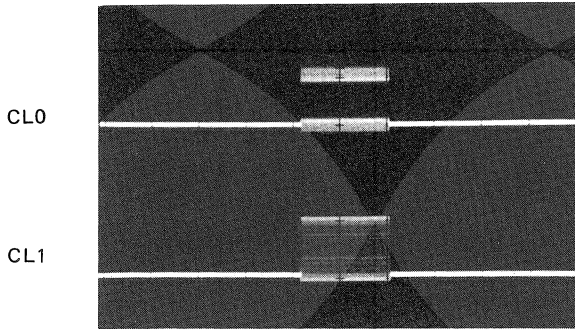


Photo 3 Waveform

d) Internal oscillator

The whole oscillating circuit has been built into the IC. The clock is supplied from TEST to X IN.

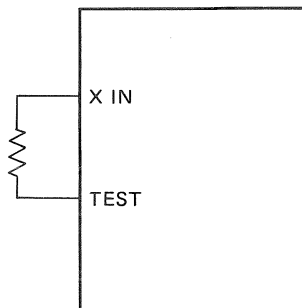


Fig. 10 Internal Oscillator with a Resistor

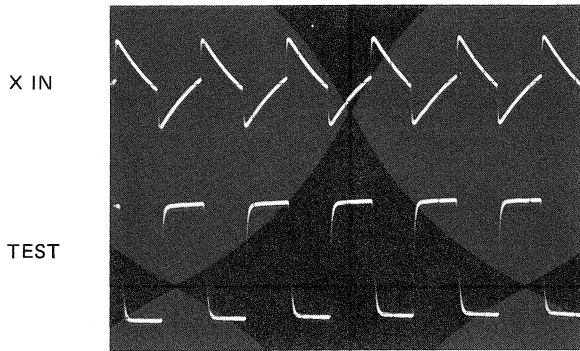


Photo 4 Waveform

e) Multiplex type oscillator

RD4023 in FEX-95

PD4023 contains (a), (b) and an IC which has no oscillator and works by receiving external lock signals. PD4023 controls the whole FEX-95 system. Check to see if clock pulses appear at each CLOCK terminal because clock timing is necessary for exchanging data.

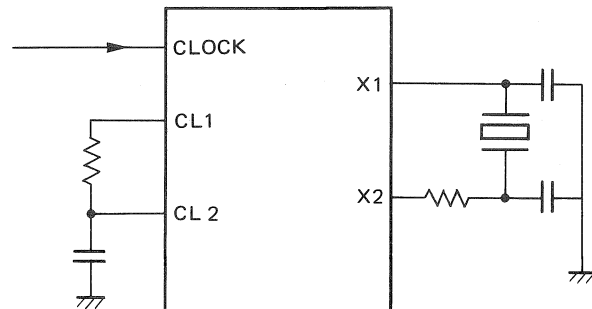


Fig. 11 Multiplex Type Oscillator

3-3 RES

A microcomputer IC has a RES (reset) terminal. This IC has internal memories. A logic circuit flip-flop in the IC works as a memory. It is necessary to reset the memories to their initial values when the power is turned on. They are usually reset by an L input. The capacitor inserted between the $\overline{\text{RES}}$ terminal and ground keeps its level low until the resetting is complete. Refer to Fig. 12. If the IC is put into operation without being reset, it may malfunction. Usually, the IC does not function until H appears at $\overline{\text{RES}}$. After resetting the memories, H level is applied from V_{DD} to $\overline{\text{RES}}$ to operate the IC. The $\overline{\text{RES}}$ terminal is shifted to L by a one-shot pulse to clear the memories, when the operation is changed. It is necessary to check the $\overline{\text{RES}}$ input because the IC malfunctions when an L signal does not come during resetting. The IC will not work if the $\overline{\text{RES}}$ is always on L.

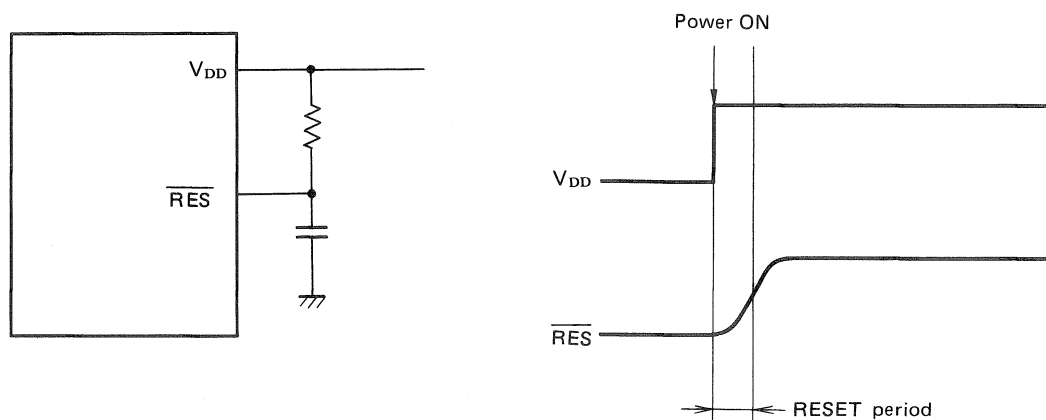


Fig. 12 Resetting by $\overline{\text{RES}}$

3-4 CS, INT

CS (chip select) and INT (interrupt) terminals are functionally similar but are inverted each other. The CS terminal is shifted to H only when a selected chip is operated. The H signal applied to CS terminal means that "The host computer is using the chip." Opposite from CS, INT keeps the IC from operating. When the INT level is H, the IC will not operate. This means that $\text{CS} = \overline{\text{INT}}$ and $\overline{\text{CS}} = \text{INT}$.

4. Measuring Equipment

Necessary equipment for troubleshooting digital ICs are shown below.

4-1 Oscilloscope

Oscilloscope is the most useful instrument for checking ICs. DC can be measured with it. With the trigger sweep type, the period of pulse width can be measured. For details, refer to No. 4 & 5, TUNING FORK. Using an oscilloscope is recommended for checking digital circuit because it often requires to observe waveform and to measure DC voltage.

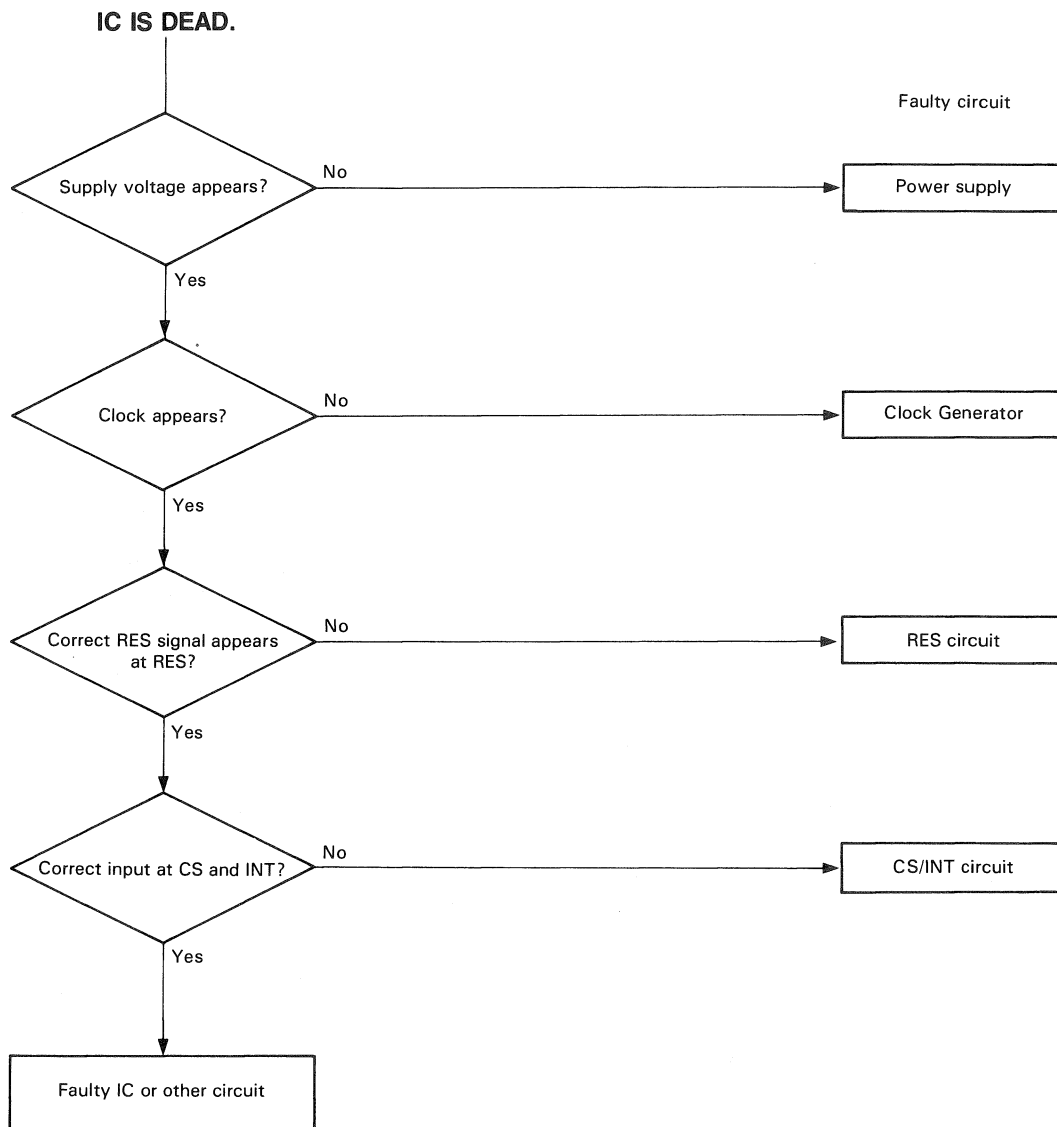
4-2 Logic Probe

This probe detects pulses and indicates H, L or other level with an LED or lamp. This is popular because of its handiness although incapable of observing waveforms. This is very useful when combined with a logic pulser or a pulse injector. Refer to DLP-50 and LPI-60, # SLH-0624, LIST OF TOOLS AND MATERIALS FOR REPAIR/SERVICE.

4-3 Multimeter

Multimeters which employ a logic probe can detect pulses and are useful for checking both digital and analog circuits.

Checking Digital ICs



5. Replacing Flat-packaged-IC

STEP-1. Cut every lead as close to package as possible to prevent the foil pattern from being torn off. See Fig. 13.

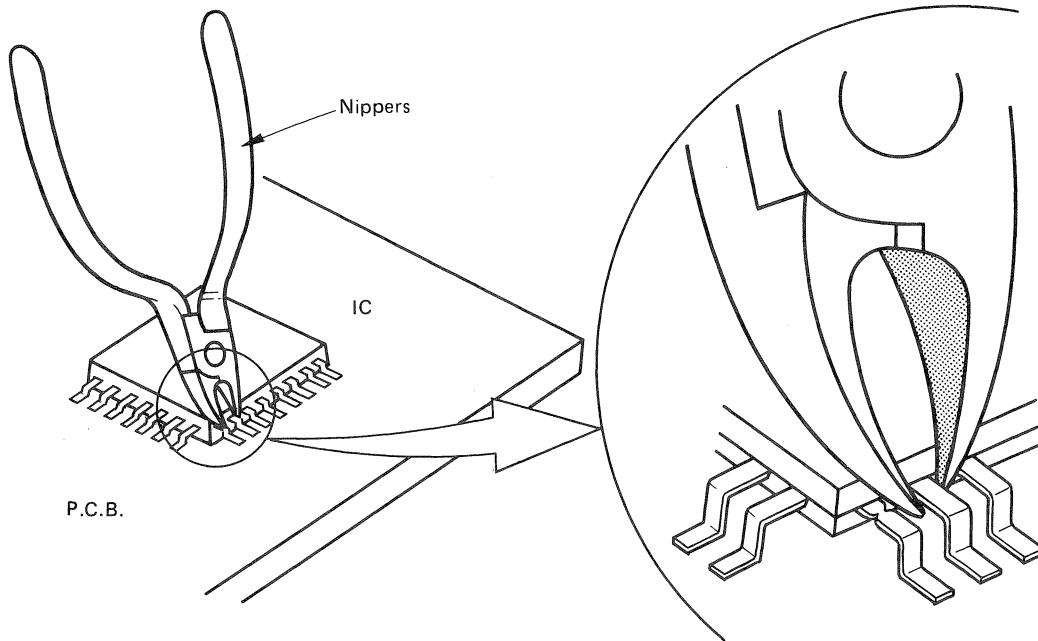


Fig. 13

STEP-2. IC's package should be left as it is to prevent the foil pattern from being turned off at this step. Melt the solder and let it flow on the leads at each side. See Fig. 14. Move the soldering iron back and forth and make a ball of solder and nipple chips. See Fig. 15. Then remove the ball. Repeat the same step at each side. Then remove IC package.

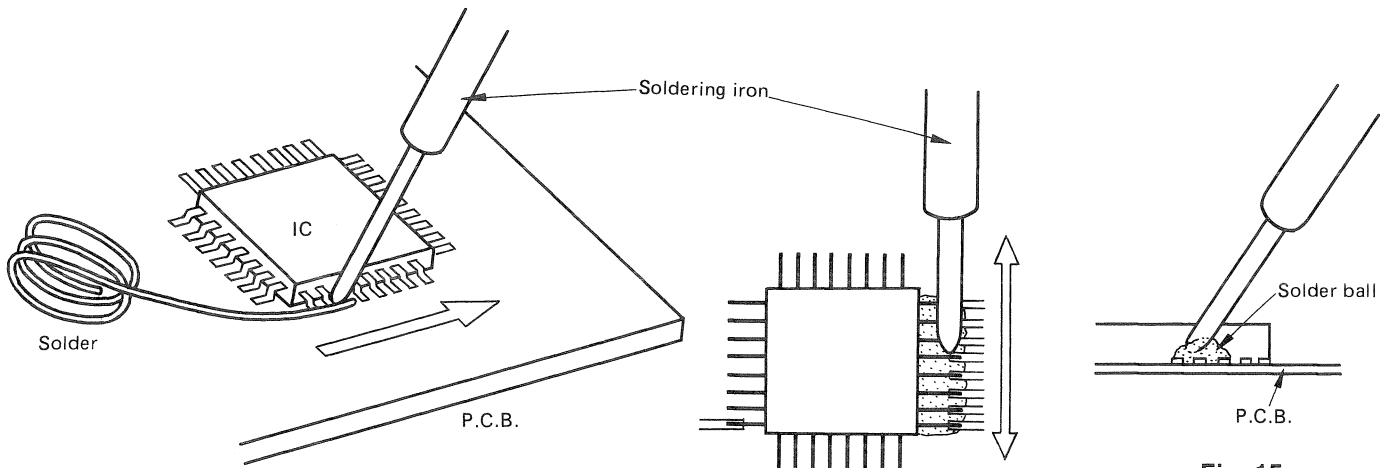


Fig. 15

Fig. 14

STEP-3. Remove solder left on the foil pattern with SOLDER REMOVING WICK (SOLDER WICK). See Fig. 16.

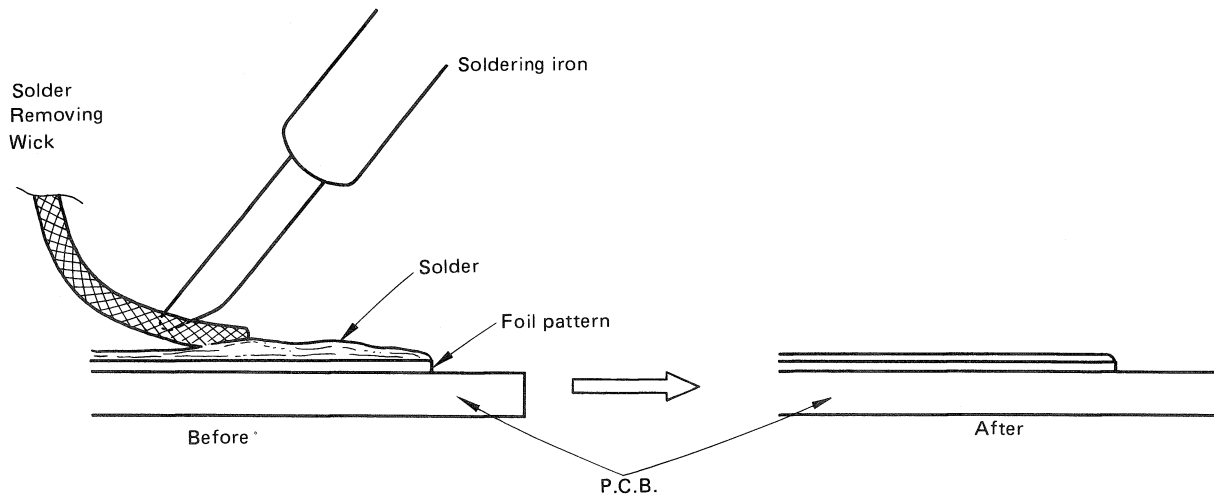


Fig. 16

STEP-4. Prepare a new IC and align all leads. See Fig. 17.

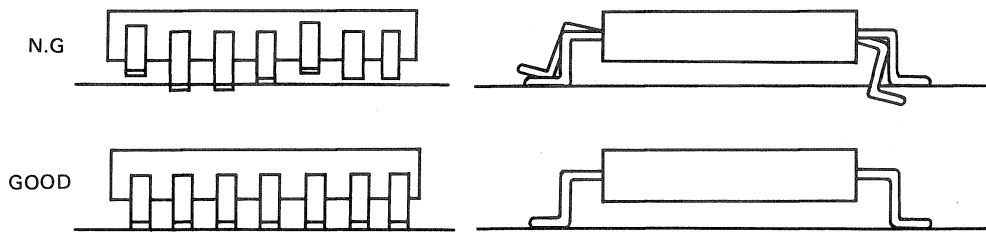


Fig. 17

STEP-5. Put the IC on P.C.Board and solder two diagonal points to mount it correctly. See Fig. 18.

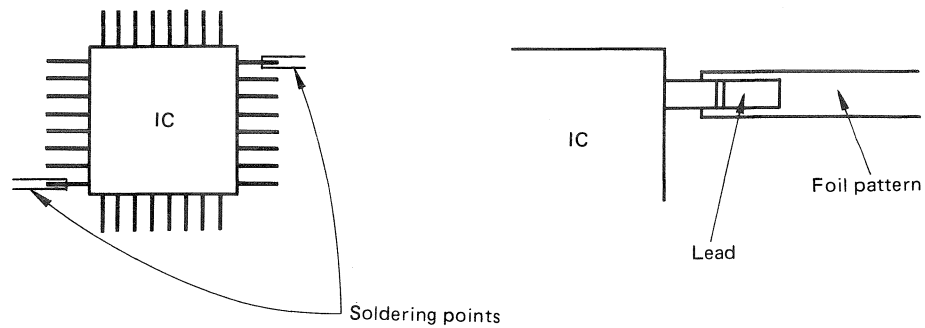


Fig. 18

STEP-6. Solder all leads. Solder bridging between leads is allowed at this step. See Fig. 19.

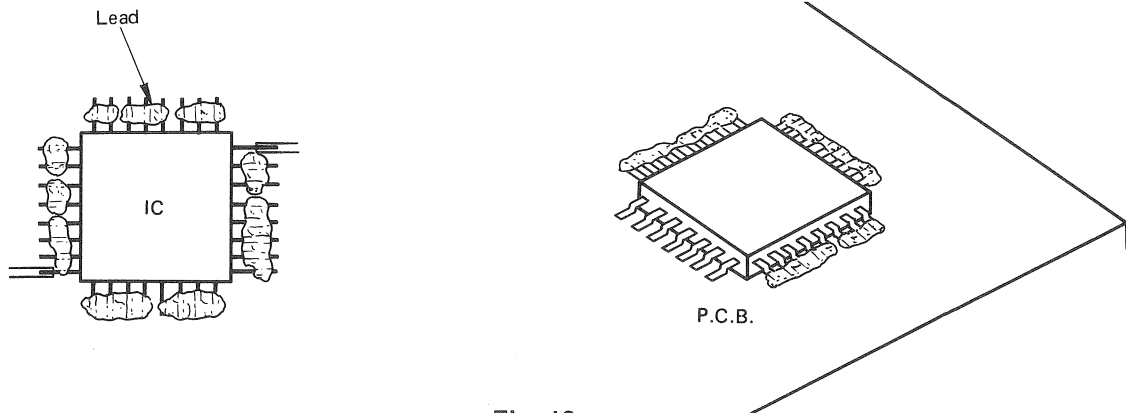


Fig. 19

STEP-7. Suck solder bridges off with SOLDER REMOVING WICK. See Fig. 20.

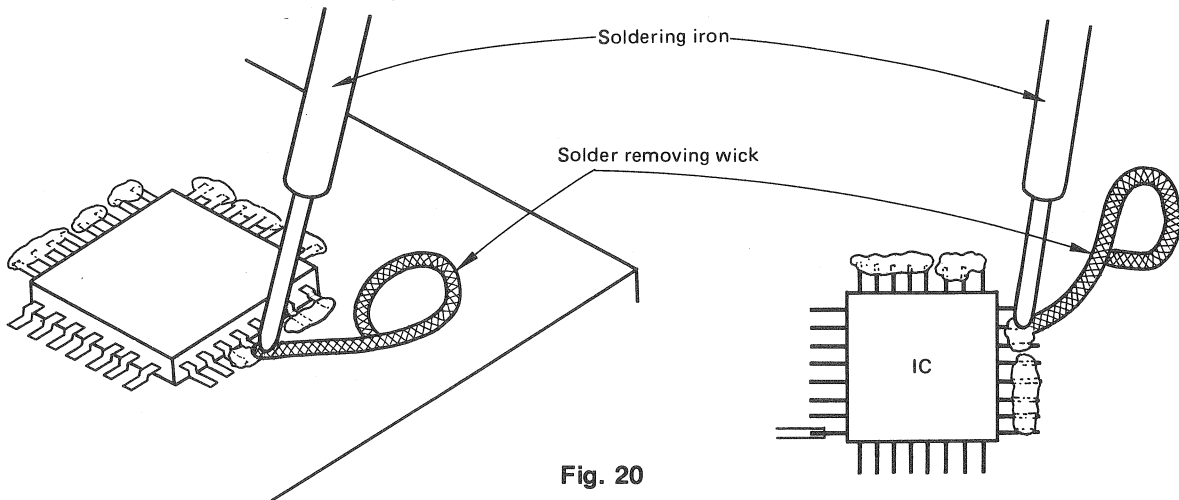


Fig. 20

STEP-8. Each lead should be re-heated by sliding the soldering iron moving it back to make the soldering sure.

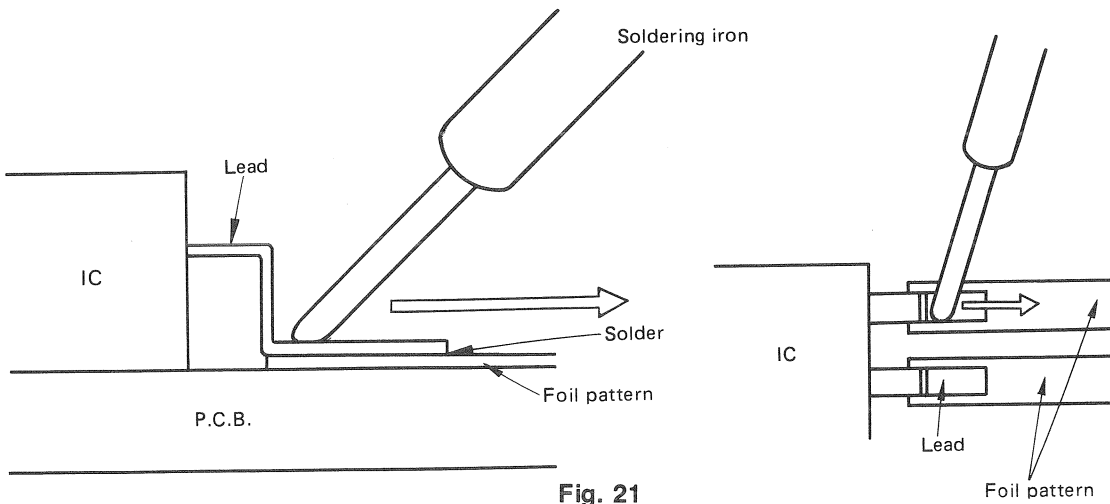


Fig. 21

Measuring Instrument

Oscilloscope (3)

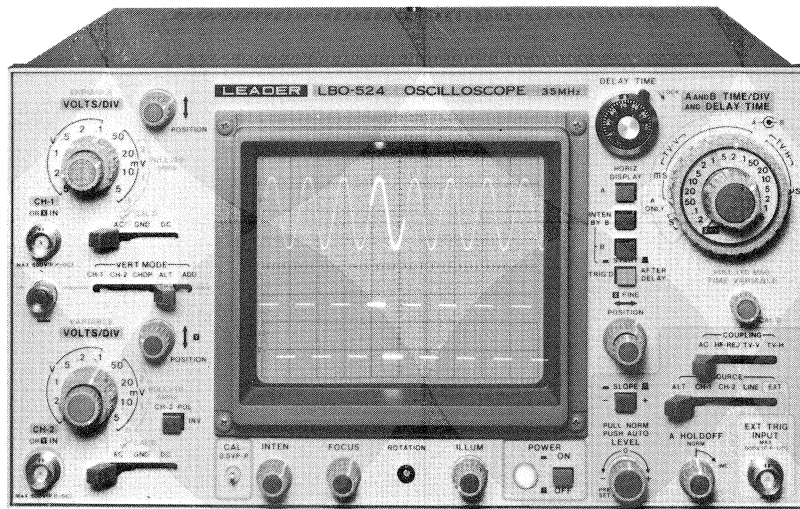


Photo 1 Triggered Sweep Oscilloscope

1. Triggered Sweep Oscilloscope

In TUNING FORK No. 5, we discussed the principles of the oscilloscope and basic methods of measuring AC/DC voltage, frequency, and phase. Unlike signals for conventional audio equipment, LD signals have complicated waveforms and a wide frequency range, and those of the Compact Disc have pulses of various widths. Such sophisticated equipment can be checked by observing the signal waveforms obtained from their circuits.

Here, we will discuss the triggered sweep (synchronized) oscilloscope, or synchroscope, which incorporates a sweep generator that provides one trace line for each input signal wave. The triggered sweep oscilloscope can automatically control sweeping frequency to synchronize with a complex input signal, whereas an oscilloscope having no

triggering circuit can only force its sweeping frequency to be an integral fraction of the input frequency.

To keep the waveform of complex signal motionless on the CRT screen, it is necessary to always synchronize the sweep signal with the input signal. It is comparatively easy to observe the distortion and frequency characteristics of an amplifier with any oscilloscope, but it is necessary to observe the rising edge of a pulse and a part of the TV composite signal when repairing LD and CD systems. An oscilloscope that has a delay circuit can expand or compress the signal width at any position to any size without deforming the waveform or shifting its phase. Fig. 1 shows a simplified block diagram of a triggered sweep oscilloscope.

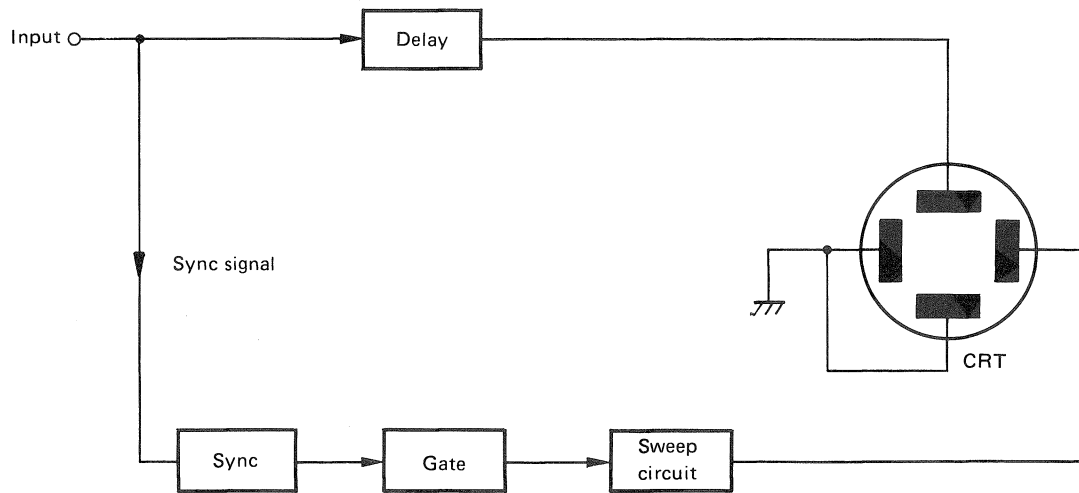


Fig. 1 Triggered Sweep Oscilloscope

Structure of Oscilloscope

The input signal should be differentiated to freeze the waveform on the screen. The differentiated pulses trigger the sweep gate that determines the starting point of saw-tooth waves. The input signal for vertical deflection should

have a delay circuit perfectly synchronized with the horizontal signal because the horizontal signals are delayed when they pass through the SYNC, GATE, and SWEEP blocks.

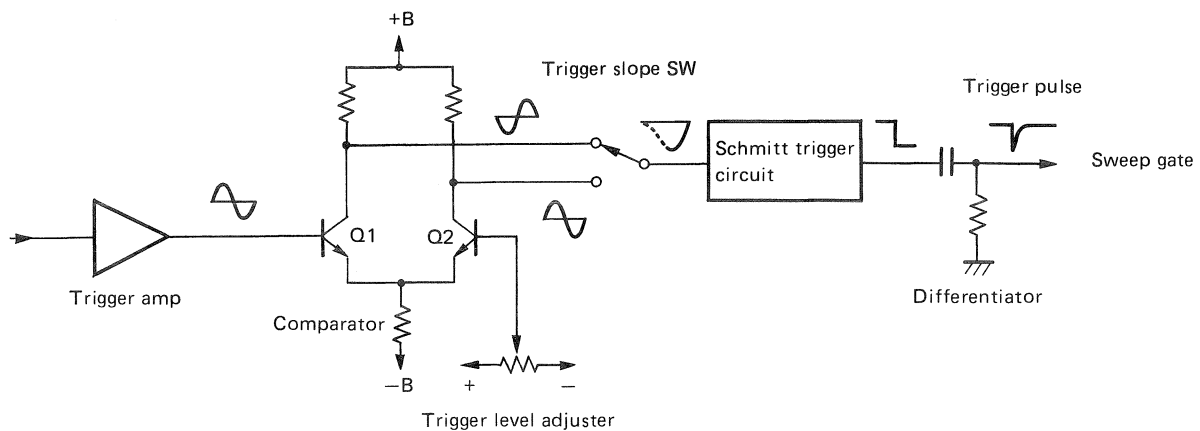


Fig. 2 Trigger Circuit

Horizontal circuit (trigger circuit)

Either the input signal or an external signal can be selected as a trigger source for the most effective and stable triggering, as shown in Fig. 3.

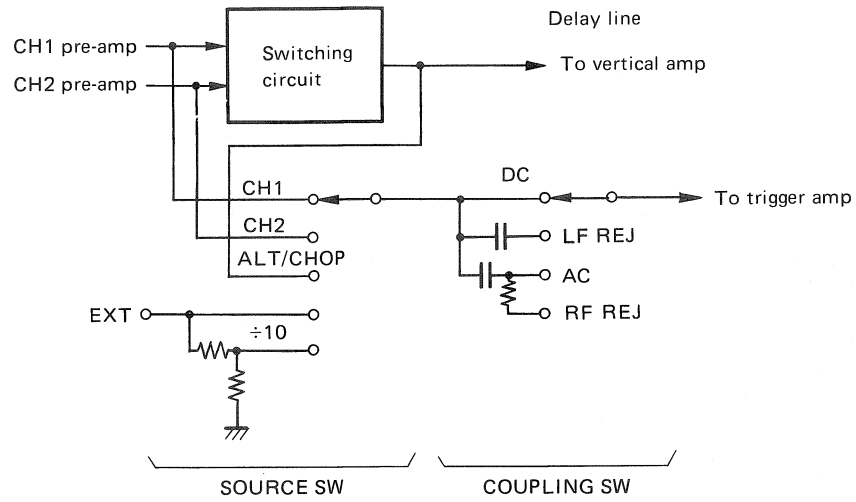


Fig. 3 Triggering Circuit

2. Dual Trace Oscilloscope

To measure the phase and amplitude difference between two input signals, it is necessary to display the two signals on the screen simultaneously. To trace two signals, two electron beam guns are required. Such a device, however, requires complicated circuitry and is expensive. Instead,

we can reduce the cost by tracing the two signals alternately with one beam, with the help of a channel-switching circuit. There are two switching systems. Fig. 4 shows the two methods: the alternating system and the chopping system.

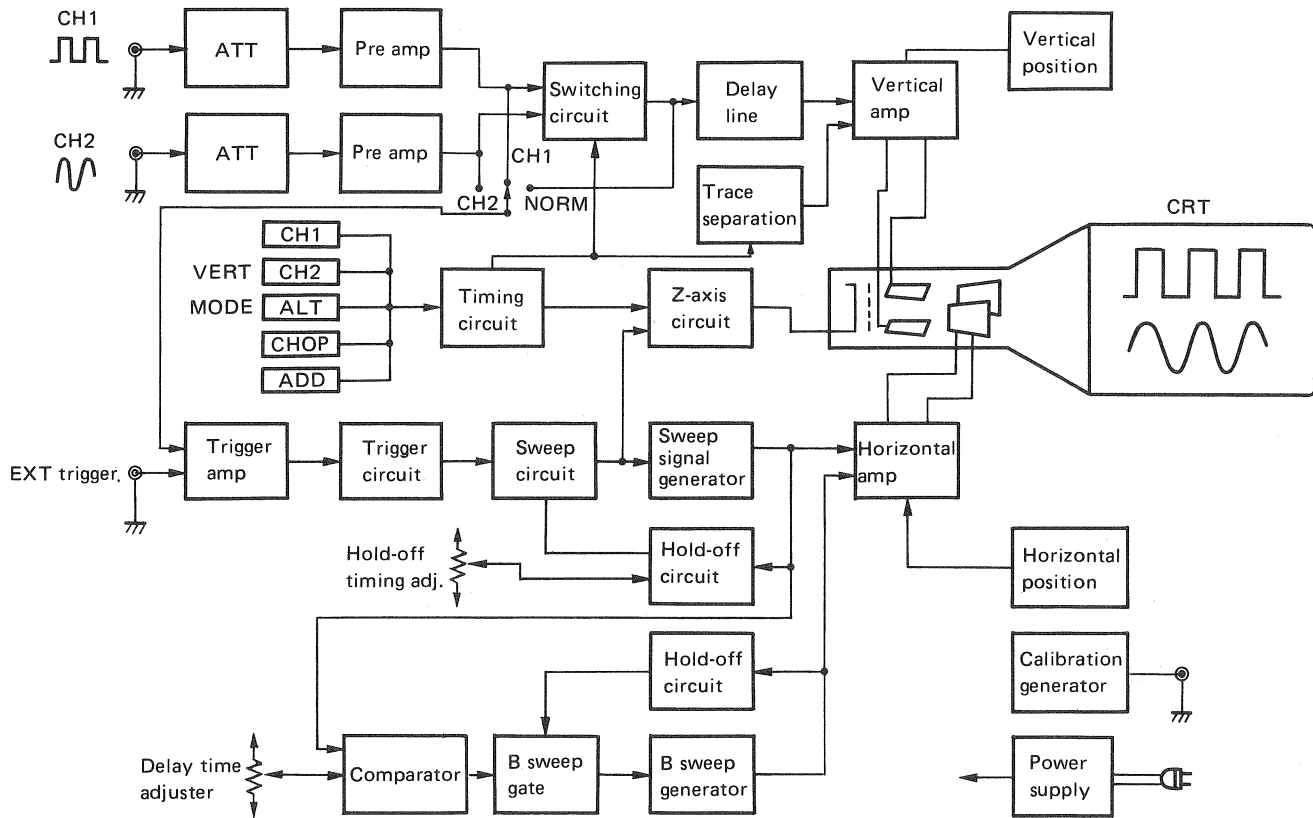


Fig. 4 Block Diagram of Dual-trace Oscilloscope

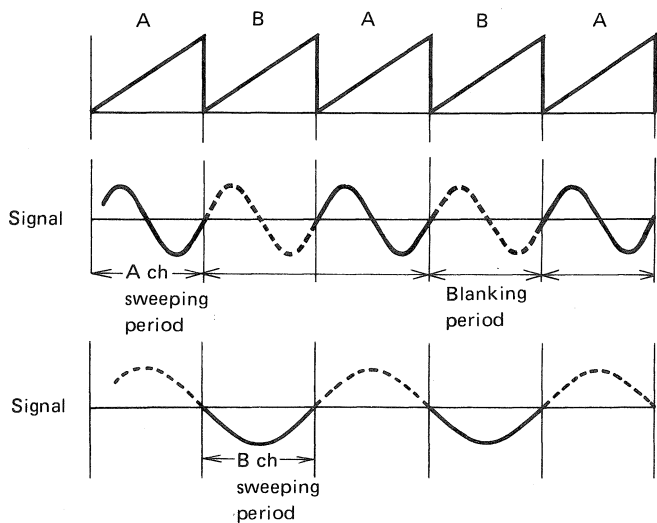
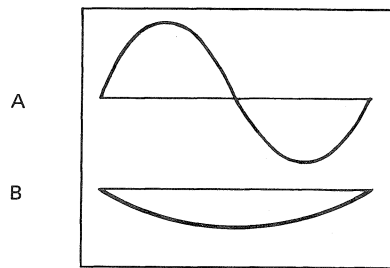


Fig. 5 ALT System

(a) Alternating (ALT) system

As shown in Fig. 5, the ALT system continuously sweeps a full trace line of one channel and then the other channel using only one beam. A switching circuit repeats this alternate operation. This means that every other wave of both channels' signals are skipped, and each trace line from one channel is delayed from the other by one tracing period. If the input frequency is low, the sweeping frequency is low, flickering increases and motionless waveforms are hard to observe. This technique is therefore suitable for observing two high-frequency periodic waveforms with a sweep period shorter than 0.1 ms; it is not suitable for observing phase difference and transient waveform.



Trace Lines of ALT System

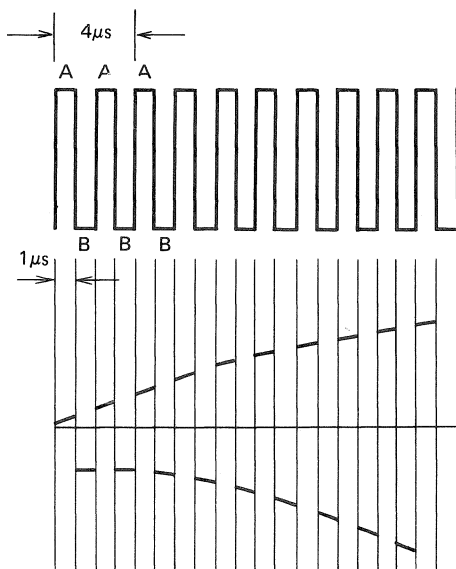


Fig. 6 Chopping System

(b) Chopping system

The both input signals are divided into many small segments by a 130 kHz switching signal. This system also skips every other segment, but segments are much shorter than a full trace line. This is suitable for observing the phase difference between the two signals, but not for high-frequency signals.

3. Principle of Delayed Sweep (Time-base Expansion)

Fig. 7 shows a block diagram of a delayed sweep circuit. The unit consists of a main sweep circuit and a delayed sweep circuit, which are similar to each other. A trigger pulse created from the input signal activates the main sweep circuit. The amplitude of the sawtooth wave sweep voltage is compared with the adjustable reference voltage that determines the starting point of delayed sweep. The starting point can be adjusted with the LEVEL control. The delayed sweep circuit is activated when both voltage values become equal. By adjusting the time constant of the

delayed sweep signal generator, one can observe an enlarged version of a desired portion of the waveform. These systems are employed in multi-trace systems, of two or more trace lines.

How to freeze the waveform

The output of the trigger amplifier is applied to the comparator. The trigger level adjuster determines the triggering level. When the input signal reaches the threshold level of the trigger circuit, the output level shifts and a trigger pulse is generated by the differentiator. The trigger signal determines the starting point of the sweep and synchronizes it with the input signal to freeze the waveform.

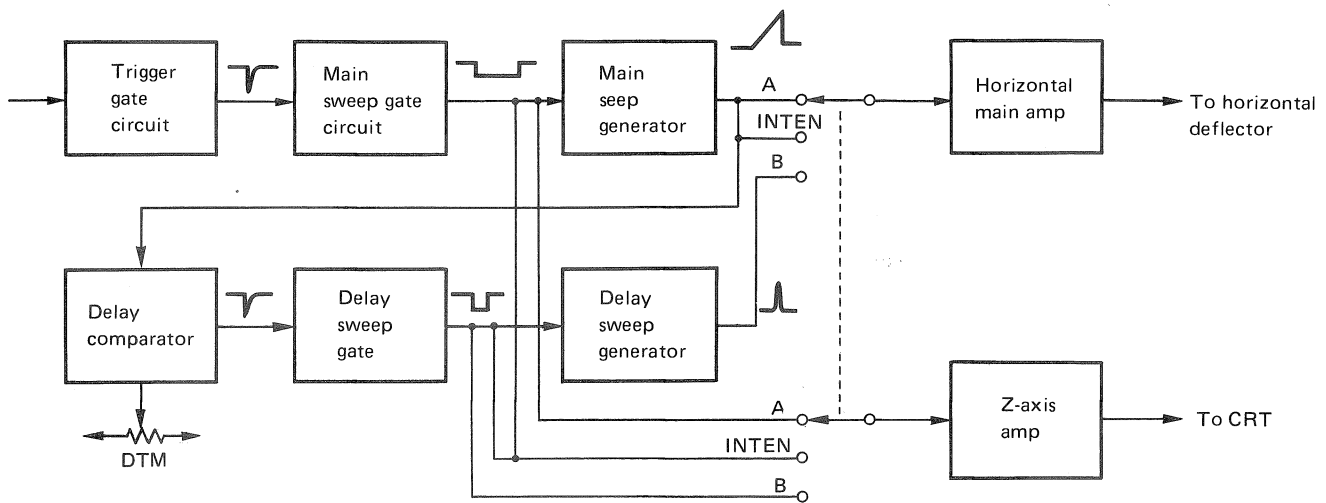


Fig. 7 Block Diagram of Delay Sweep Circuit

4. Sawtooth Wave Generator

The sawtooth wave signal deflects the beam horizontally to trace the vertically deflecting input signal. When the sweep gate circuit receives a trigger pulse, it puts out L. The sweep generator starts putting out a sweep signal. The level of the sawtooth wave should return to zero when tracing is finished. The hold-off circuit negatively feeds back its output voltage to make the beam return to the starting point when the sawtooth wave rises to a certain point. The circuit also keeps the sweep-gate circuit inactive until the beam finished tracing a full wave. The vertical input signal is delayed in order to synchronize with the delayed sweep signal. The sweep signal and input signal are applied to the horizontal and vertical deflection circuits of the CRT.

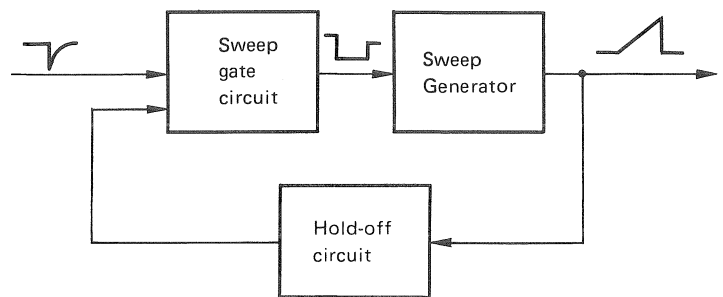


Fig. 8 Sawtooth Wave Generator

5. Measuring Method

(a) Measuring the peak voltage of DC + AC signal
 DC and GND positions are selected when measuring a fluctuating DC (DC + AC) signal. If 0.2 V/division is selected, the input waveform will be as shown below. When the

DC component is much larger than the AC component, it is better to measure the DC component and AC component separately.

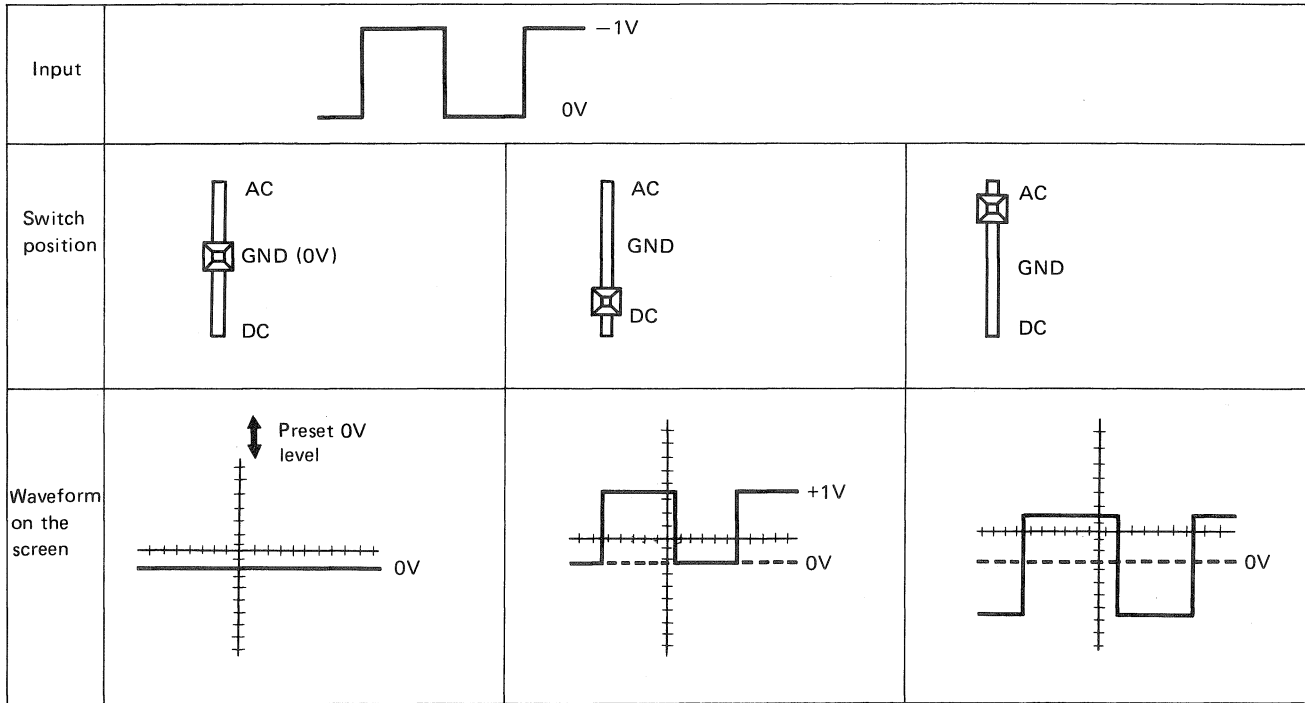


Fig. 9 Peak Voltage

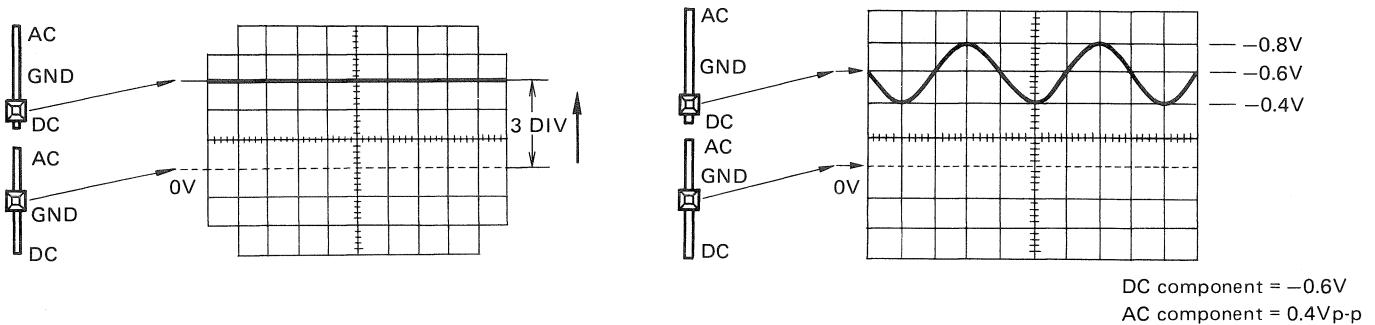


Fig. 10 Measuring the Peak Voltage of DC + AC

(b) Dual trace

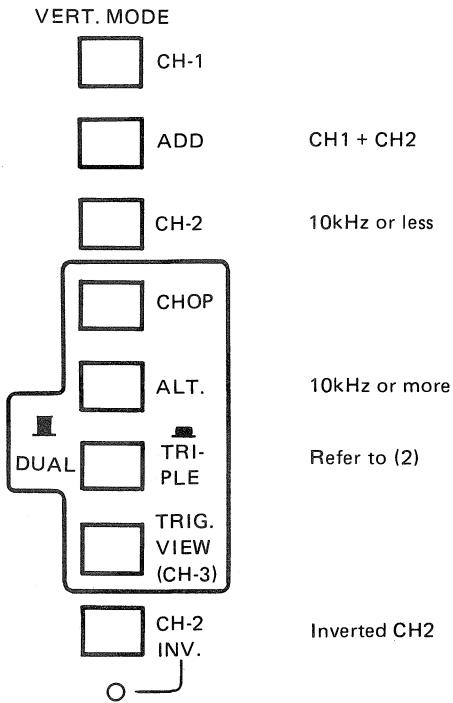
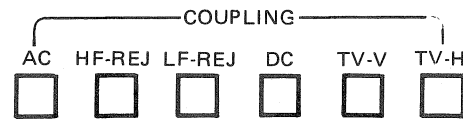


Fig. 11 Vertical Mode

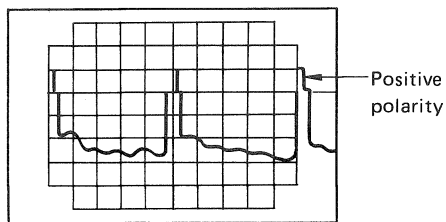
(c) TV-V, TV-H

The vertical sync signal is extracted from the composite video signal and the sweeping frequency is synchronized to the vertical sync signal when TV-V is selected. The sweep frequency is synchronized with the horizontal sync signal when TV H is selected.

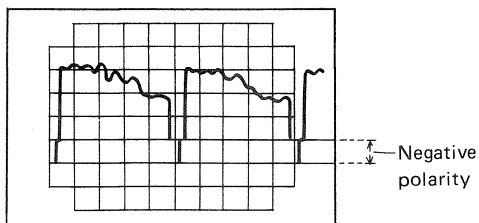


COUPLINGG

- AC 10Hz – 50MHz
- HF-REJ High frequency rejection 10 – 20kHz
- LF-REJ Low frequency rejection 5kHz
- DC 0 – 50MHz
- TV-V Synchronized to TV vertical signal
- TV-H Synchronized to TV horizontal signal



SLOPE +

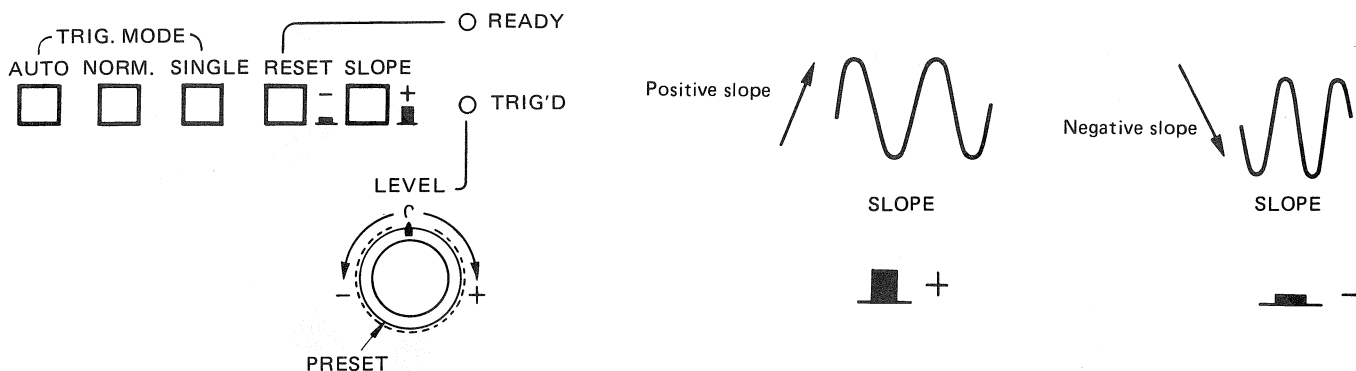


SLOPE -

Fig. 12 Coupling Circuit

(d) SLOPE shifting

The slope of a signal can be selected as follows: To trigger on the rising slope of the signal, release the SLOPE, push button; to trigger on the falling slope, push it in.



TRIG. MODE

- AUTO Self triggering when the trigger signal made from input signal disappears
- NORM..... Synchronizes to input signal
- PRERESET The triggering level comes to the mean level
- SLOPE..... Signal polarity

Fig. 13 Trigger Mode

(e) LEVEL (trigger level adjustment)

This determines the starting point of the trigger. If the level goes out of the range of the input signal level fluctuation, the lamp turns off, and synchronization becomes impossible.

The starting point depends on the trigger level.

PRESET (Turn counterclockwise): The level is preliminarily set at the center of the waveform.

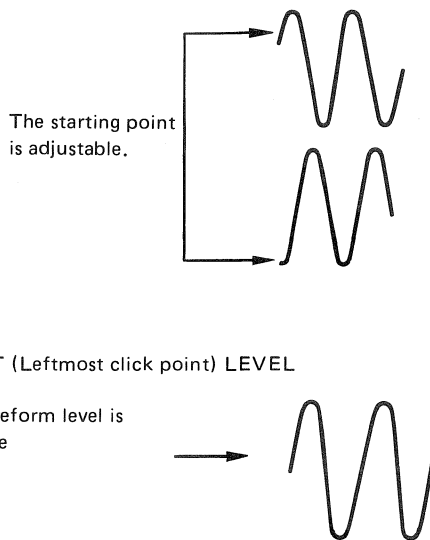


Fig. 14

6. How to Expand the Waveform

- a) Select A, HORIZ DISPLAY SW.
- b) Display waveform.
- c) Adjust TRIGGER LEVEL to make the waveform motionless and clear.
- d) Select A INTEN, HORIZ DISPLAY.
- e) Turn the INTEN control slowly counterclockwise. You will find part of the waveform brighter than the other part.
- f) Turn DELAY TIME until the bright part reaches the area you want to enlarge.
- g) Turn B TIME/DIV and determine the width of the bright part to be enlarged. When observing a video waveform, set B TIME/DIV at 10 μ s.
- h) Select B, HORIZ DISPLAY.
- i) Adjust INTEN for optimum brightness.

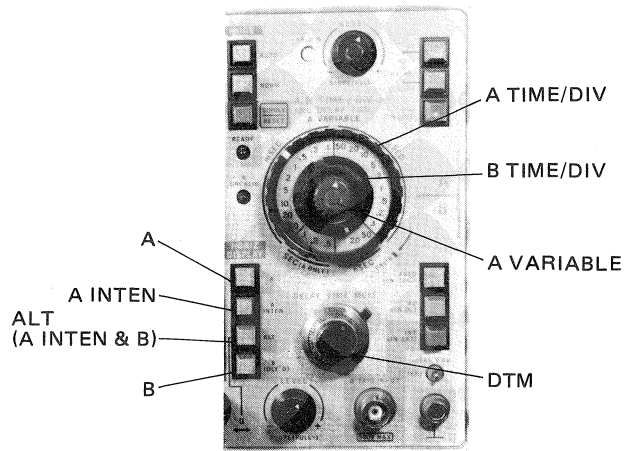
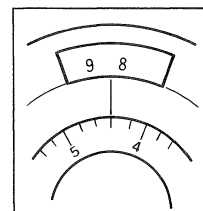
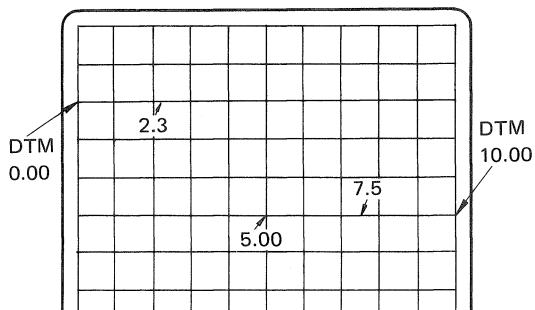


Photo 2

Delay Time Multiplier (DTM) indicates the time with three figures. First read the right number in the window, then the dial scale below the cursor. The following figure indicates 8.44. The unit ms or μ s depends on the TIME/DIV scale.



Delayed sweep time = A sweep time \times DTM reading

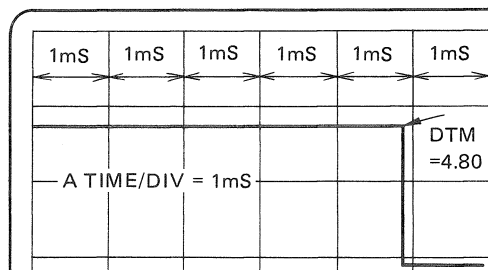


Fig. 15 Reading Delay Time

Wave Observation by Delayed Sweep
Normal Display, CH1 and A Mode

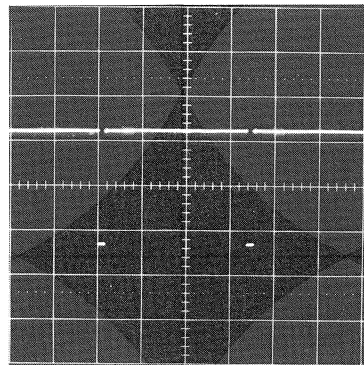
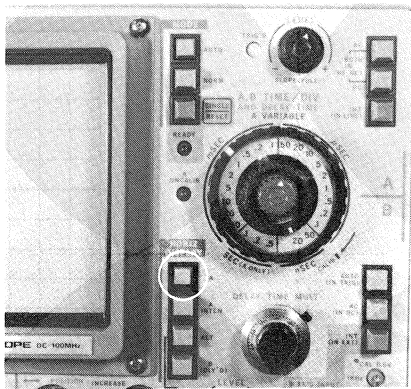


Photo 3 A Waveform at A TIME/DIV:1 mS/DIV

A Intensity and 0V Delay Time

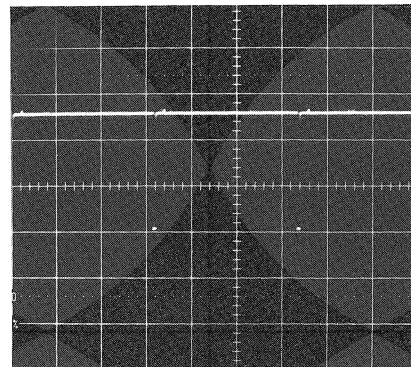
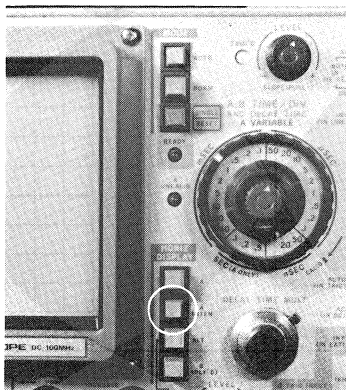


Photo 4 A TIME/DIV: 0.1mS, B: 2 μ S
 The trace line starts from the 0V level because the delay time is 0.

Varying B SWEEP at A INTEN

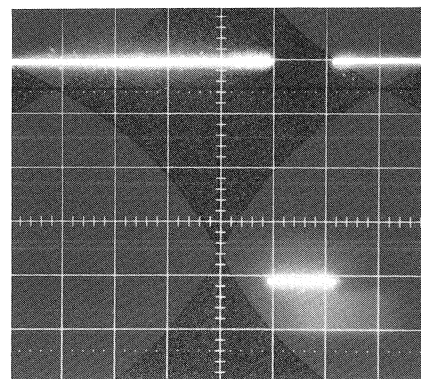
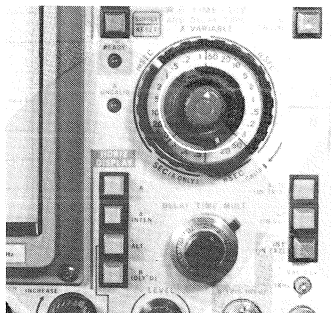


Photo 5 A: 0.1 ms, B SWEEP: 50 μ s
 Half of the trace line becomes bright because A is 0.1ms, B SWEEP is 50 μ s and DTM is 0.

Increasing DELAY TIME at A INTEN

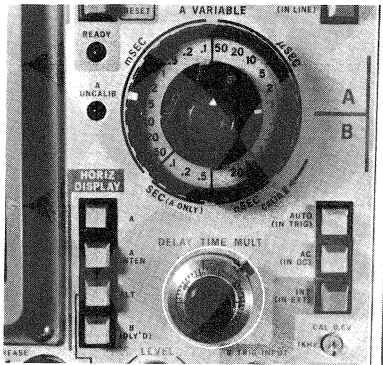
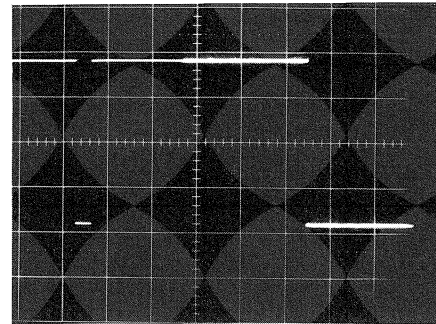


Photo 6

Bright portion moves rightward as DELAY TIME is turned clockwise. Now the DELAY TIME reads 4.1 and B



SWEEP has been delayed by 4.1ms ($0.1\text{ms}/\text{DIV} \times 4.1$).

B Display

Photo 7 shows the enlarged B at the time the HORIZONTAL DISPLAY B is depressed. Turn the B SWEEP clockwise to enlarge the waveform horizontally.

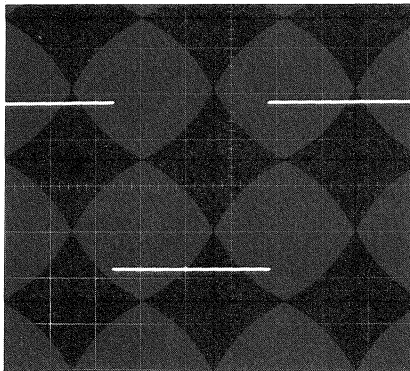


Photo 7

Quality Information System (4)

Accuracy Makes High Quality Products

Products that passed factory inspection may be rejected by users. The object of Quality Control (QC) is “providing consumers with products that satisfy their needs.”

1. Inspection and Test

Many people think that the job of QC is to inspect and test products. If the field failure of products is high, they may blame the inspectors. The task of inspection and test are only a part of QC. Regular inspection and test are conducted under stipulated conditions. If these conditions are different from those of actual use, however, QC cannot assure product quality. Analyses of quality information (QI) often show that there were many problems not prevented by inspection and test.

2. Importance of QI

What shall be done if quality assurance cannot be accomplished by inspection and test only? Analyzing field QI as much as possible is the third necessity. Collecting and analyzing QI, finding points to be improved and taking countermeasures are basic QC activities. Specifications and

test conditions shall be changed according to users' needs. We have to avoid repeating the same problems already experienced. Although the QI obtained inside the factory is useful, field QI is indispensable to know the users' demands for improvement.

3. What will Happen if we Receive Improper QI?

If quality assurance is carried out only by collecting and analyzing QI, insufficient and incorrect QI will lead to misunderstanding and inadequate improvement. This is unnecessary and may even be injurious. It is useless even if it involves no problems. With such QI, no resolution of the problems can be obtained, and all efforts of the reporters and investigators will be in vain. It is comparatively easy to investigate whether QI obtained inside the factory is correct or not. On the other hand, it takes a long time to contact the reporters and confirm the contents of QI received from the field.

* NOTE : PLEASE DON'T FORGET TO WRITE THE FOLLOWING

1. CLASSIFICATION

The importance of your problem by ticking the corresponding blank classified as follows:

- ☆ The defect which may be possibly corrected in the future product.
- ☆☆ The defect which may grow a serious problem and is required to be corrected in the near future production.
- ☆☆☆ The defect which is creating a serious problem and requires immediate countermeasure on all units including stock.

2. SYMPTOM AND CAUSE

Failure conditions, probable causes, etc. In detail as much as possible.

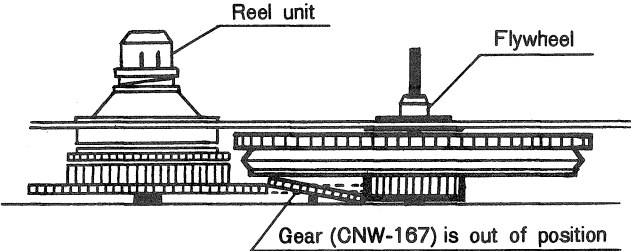

3. REQUESTED ACTION

The action to be taken to solve the problem. Also your suggested countermeasures and comments, if any.

THANK YOU

PIONEER QUALITY INFORMATION

* CLASSIFICATION --Note-1		
	X	
☆	☆☆	☆☆☆

MODEL KE-6000	SUFFIX E	SUBJECT Gear is out of position	Date Aug. 18 '84
* MALFUNCTION (Symptom, Enviromental condition, etc.)--Note-2 Mechanical noise. Reel unit does not turn.			Ref. No. SSV-1105
 <p>Reel unit</p> <p>Flywheel</p> <p>Gear (CNW-167) is out of position</p>			Company Name ABC Sound Co
			Place Tokyo
* CAUSE/REMEDY (Your Request, Suggestion, Failure trend, comment, etc.) Note-3 Too much gap on the axis of the gear so that the gear comes out of its position. When gears are not engaged together, the reel unit (CXC-177) does not turn synchronised with flywheel. By putting a washer the gears are engaged and gear noise is also eliminated. Please make gear diameter a little bit wider.			Issued by K. Yamada
			Approved by 
			PROBLEM POINTED OUT BY
			X End user X Retailer
			- Distributor Other
			Quantity 3 pcs.
			SERIAL NO.
			DK28524
			DL26554
			DL26892
			X Sample Q'ty 5 pcs.
			Photograph
			- Enclosed X Separately
			Other
			SALES STARTED Oct. 1983
			CUMULATIVE SALES Q'TY 1,534 pcs.
COMMENT OF YOUR SALES DEPARTMENT (Reaction of customers, Effect on sales, etc.)			
This symptom is also pointed out by our three dealers, we would like you to take a prompt action before this problem becomes serious.			

A New Example of Quality Information

Please produce QI referring to this example.

4. Examples of Field QI Liable to be Misunderstood

In the following cases, the factory cannot take appropriate counteraction in response to the claims due to insufficient or improper QI.

Example 1: The quality of XX-0000 (model name) is poor. Received 10 claims.
(For lack of detail, factory cannot determine what is wrong with the product.)

Example 2: YY-0000 (model name) is noisy. We can no longer sell this model.
(Because the noise level of this model is equal to that of the other conventional models, our factory cannot understand the problem. We would like to know the loudness, external interference, time of day, failure rate, etc. and whose opinion it is; dealers' or your quality inspectors'. Without such information, the factory may assume that the claim might have been posted by a customer who was using the model under unexpected conditions.)
The factory will be confused when the performance or quality of new products which have been inspected on the same level and shipped out under the same conditions as those of conventional ones, is said to be poor without detailed information. A model marketed worldwide may not be accepted in some particular area. Identifying problems is impossible without knowing the situation and the reason for user's rejection.

5. What is Accurate QI?

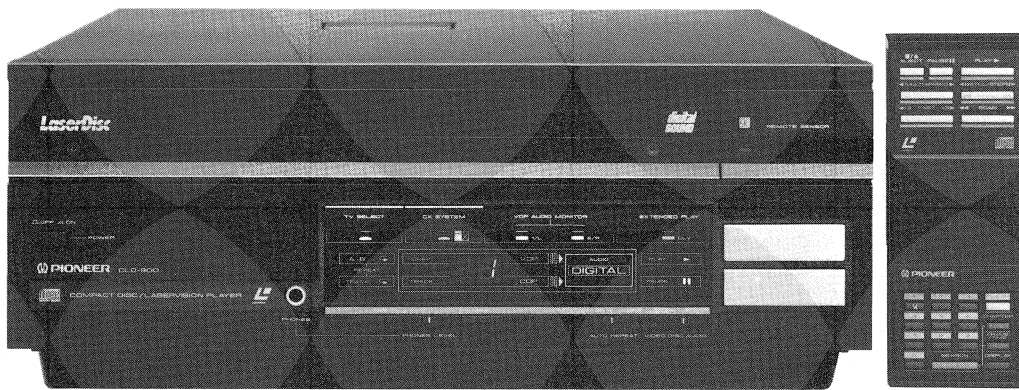
The most important element of QI is accuracy. Accurate QI should be based on raw data reflecting no personal bias. If it takes too long to obtain detailed information, we will not be able to take prompt action. When reporting QI, please consider the following for producing accurate QI:

- Observe symptoms objectively and eliminate assumptions and opinions of the reporter from the fact. (Assumption and opinion are to be headed by "My presumption" and "My opinion.")
- Clarify source of QI. (Example, "Our dealer claimed," "our inspector found," etc.)
- Fill in all blanks of the QI form. (Unknown items are to be described as "unknown." This will help us distinguish useful information from unknown points.)

6. Controlling QI is an Important Part of TQC (Total Quality Control)

When accurate QI are collected inside the factory and from the field worldwide, QC will function well and will result in product quality improvement.

Please note that accuracy of QI is far more important than quantity of QI.



CLD-900



LaserVision-Compact Disc compatible player (NTSC type) scheduled to be introduced into the market early next year. This is also capable to play an LDD disc or LaserVision disc which has digital sound information in addition to analogue picture and sound information. Refer to page 74.

New Product

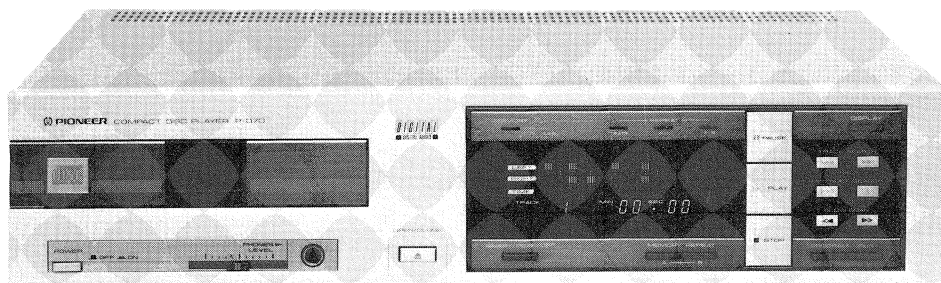
Compact Disc (CD) System

1. Compact Disc (CD) System and LaserVision System

In the last issue we discussed the LaserVision (LV) System (LD-1100). Here, we will discuss the basic principle of the Compact Disc (CD) System, which was jointly developed by Sony and Philips, basing on our new model, P-D70.

The CD System is a totally new precision digital audio disc system. It produces a very high quality sound, far superior to conventional analog audio systems. Because the CD system is based upon the same principles as the LV System, these two systems have many common features.

In both systems, disc material is plastic, information is recorded in the pattern of pits, and a laser beam is employed in the cutting and pickup systems. The focus, tracking and radial servo systems are almost the same. Refer to "LaserDisc™ System" (TUNING FORK No. 6) for information regarding the optical cutting and pickup mechanisms and refer to the operating and service manuals for information regarding operation, adjustment, and detailed circuit descriptions.



P-D70

There are, of course, some differences between the LD-1100 and P-D70. The P-D70 has no tracking mirror for deflecting the laser beam. Instead, it has a tracking coil, which moves the objective lens parallel to the disc surface. This is, however, not the difference of system itself.

Instead of a tangential mirror, the P-D70 has a random access memory (RAM) reservoir, which outputs information at a constant speed.

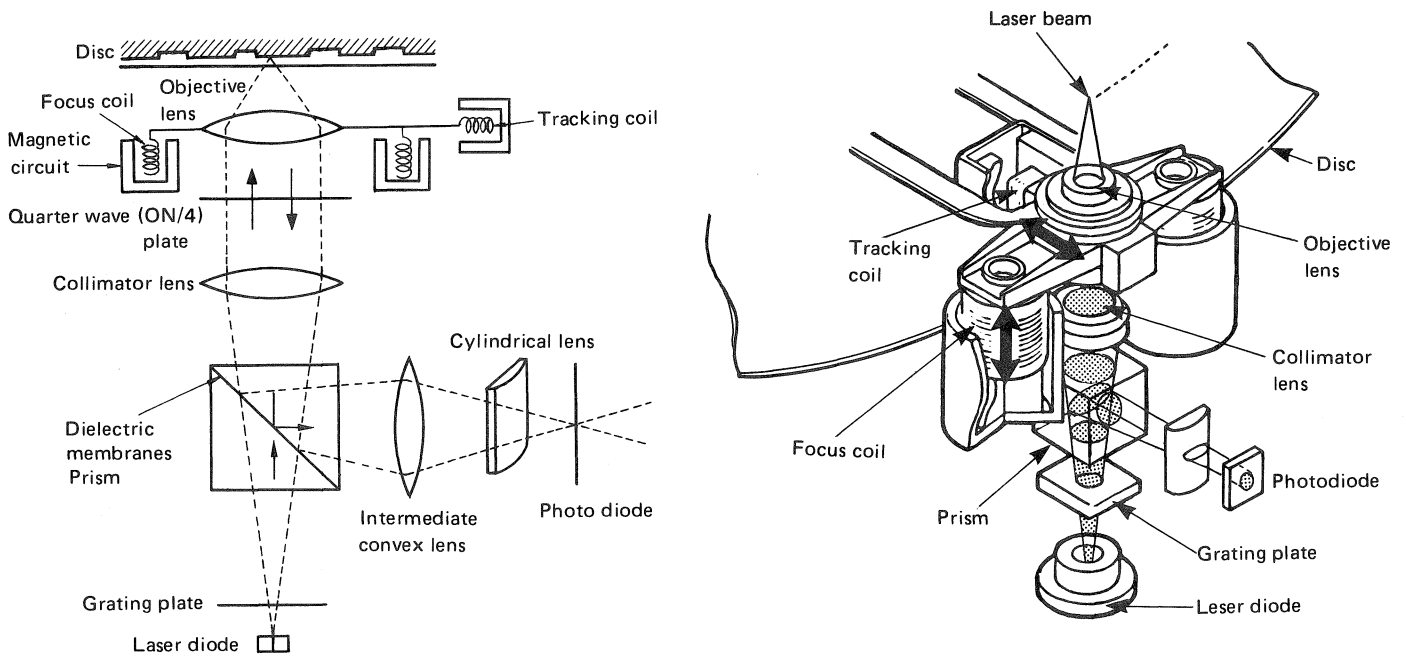


Fig. 1 Optical Pickup System

Fig. 2 shows the CD size. Information is recorded on one side only. A label bearing the contents is attached on the other side. The CD and LV systems also differ with regard to speed. The CD is Constant Linear Velocity (CLV) type. Playing time is approximately 60 minutes (75 minutes max.) at a linear speed of 1.2 m–1.4 m/sec (speed varies from 500 r.p.m. on the innermost lead-in track to 200 r.p.m. on the outermost lead-out track). The speed of the LV CLV disc varies from 1800 r.p.m. to 600 r.p.m. (about 11 m/sec). The recorded signal frequency spectrum of the CD system ranges from 0 Hz to 2 MHz, while that of the LV system ranges from 2 MHz to 14 MHz.

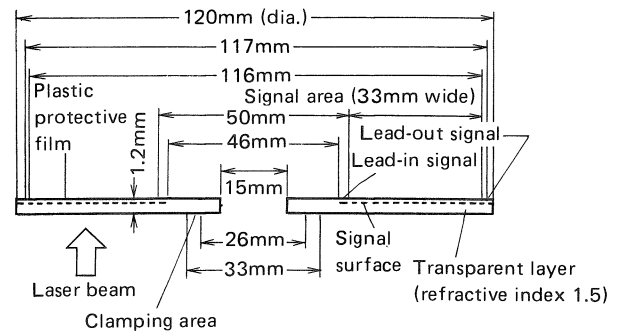
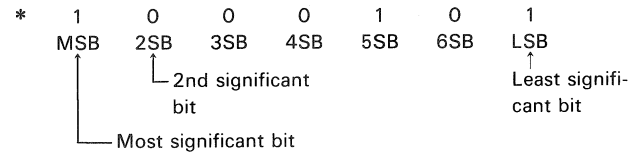


Fig. 2 CD Dimensions

The biggest difference between the CD and LV systems is the signal processing method. In the CD system audio signal samples are taken frequently (44,100 times/sec) and converted into binary pulse codes* (Pulse-code Modulation (PCM)). The right (R) and left (L) codes are then aligned on a single stream and scrambled in a programmed order. Parity codes* are then added, and the disc is cut in the same way as in the LV system.

*Binary code system: A system of mathematical computation based on powers of 2. 0 and 1 are used to represent the binary conditions ON and OFF respectively.

2's complement is suitable for representing negative values by assigning "1" to the MSB.*
 Negative count down is a subtractive process from the highest number.



Analog signal	Decimal number	Binary number	Binary waveform
	Quantized level	2's complement	
	+7	0 1 1 1	
	+6	0 1 1 0	
	+5	0 1 0 1	
	+4	0 1 0 0	
	+3	0 0 1 1	
	+2	0 0 1 0	
	+1	0 0 0 1	
	0	0 0 0 0	
	-1	1 1 1 1	
	-2	1 1 1 0	
	-3	1 1 0 1	
	-4	1 1 0 0	
	-5	1 0 1 1	
	-6	1 0 1 0	
	-7	1 0 0 1	
-8	1 0 0 0		

Fig. 3 Decimal Values to 4-bit Binary Codes

The information (signal) recorded on a CD is digital while that recorded on an LV disc (LVD) is analog. In the LV system, pit length varies continuously in relation to the length of the FM wave carrying the composite picture and sound information. On the other hand, in the CD system, there are only 9 pit lengths. Refer to Fig. 4.

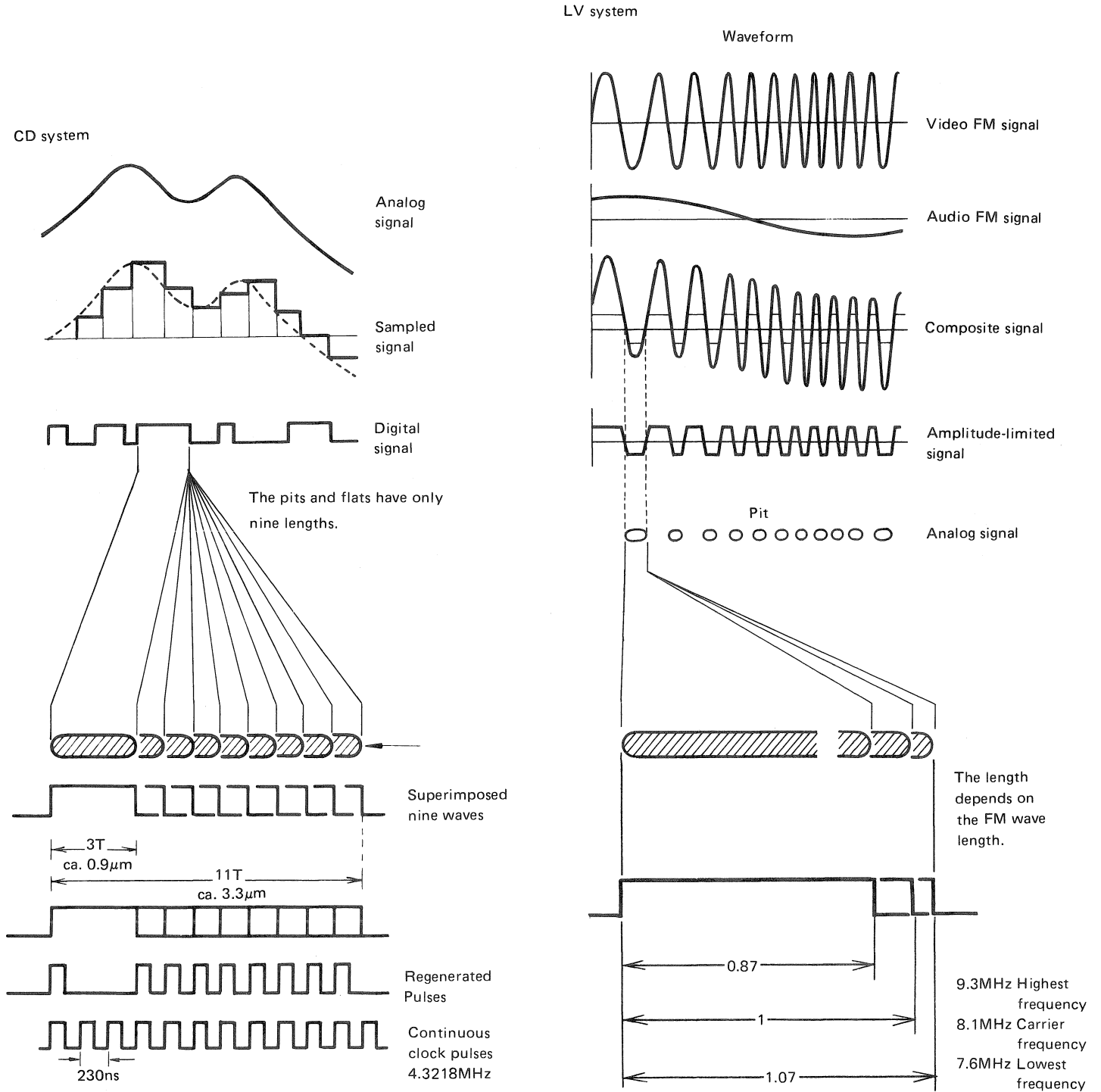


Fig. 4 LV and CD Pit Lengths

This digital processing method provides excellent sound quality: wide dynamic range, low distortion, flat frequency response and immeasurably low wow and flutter. Table 1 compares the specifications of the CD system with those of LP analog phonogram system.

Specifications	CD	LP
Frequency response	5 Hz – 20 kHz ± 0.5 dB	30 Hz – 20 kHz ± 3 dB
Dynamic range	More than 95 dB	Less than 55 dB (1 kHz)
S/N ratio	More than 95 dB (1 kHz)	25 – 35 dB
Channel separation	More than 90 dB (1 kHz)	Less than 60 dB
Harmonic distortion	Less than 0.004% (1 kHz, 0 dB)	0.2%
Wow & flutter	0 (Quartz accuracy)	0.03%
Playing time	Approx 60 min (75 min max) recorded on one side only	20 – 25 min/side
Revolution	1.2m – 1.4m/sec, CLV, approx 500 – 200 rpm, counterclockwise	33 1/3 rpm, CAV, clockwise
Tracking	Outwardly from inside	Inwardly from outer groove
Service life	Semi-permanent	HF response decreases after playing 10 – 20H
Material	Acryl/polycarbonate resin	Polyvinyl chloride (PVC)
Pickup	780 ± 10 nm laser semiconductor	Cartridge/stylus

Other specifications of the CD system

Sampling frequency:	44.1 kHz
Sampling order:	Simultaneous
Quantization:	16-bit linear/channel
Modulation:	8-to-14 modulation (EFM)
Coding:	2's complement
Error correction:	Cross-interleave Reed Solomon Code (CIRC)
Redandancy:	30.6%
Preemphasis:	No or 50/15 μsec
Transfer rate:	2.03M-bit/sec before EFM 4.3218 MHz after EFM
Pit Physical depth:	0.11 μm
Effective depth:	0.165 μm
Length:	0.9 – 3.3 μm
Width:	0.5 μm
Track pitch:	1.6 ± 0.1 μm

Table 1 Specifications of CD and LP Systems

Fig. 5 shows the simplified process of recording and playback of the CD system.

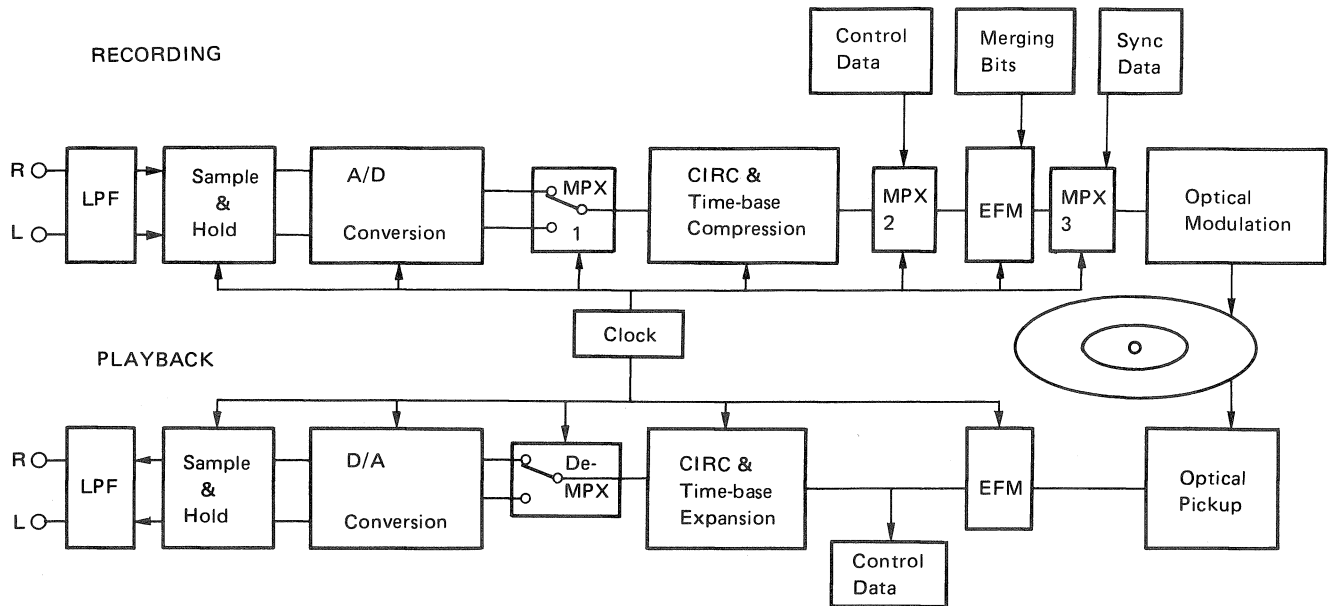


Fig. 5a. Block Diagram of Recorder and Player

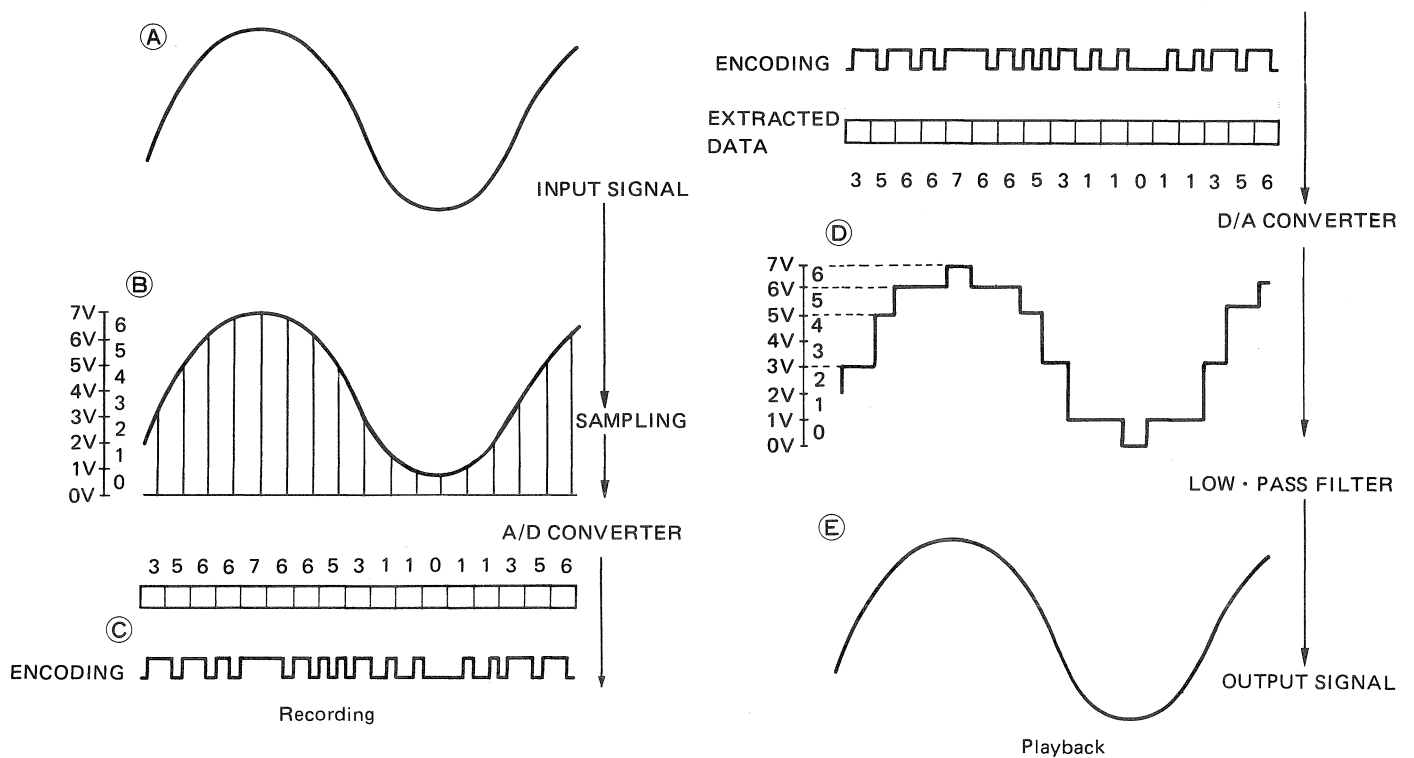


Fig. 5b. Conversion from Analog-to-Digital and Vice Versa

2. Recording Process

Let's see how the audio signals are recorded. The recorder processes the sampled data in the following order.

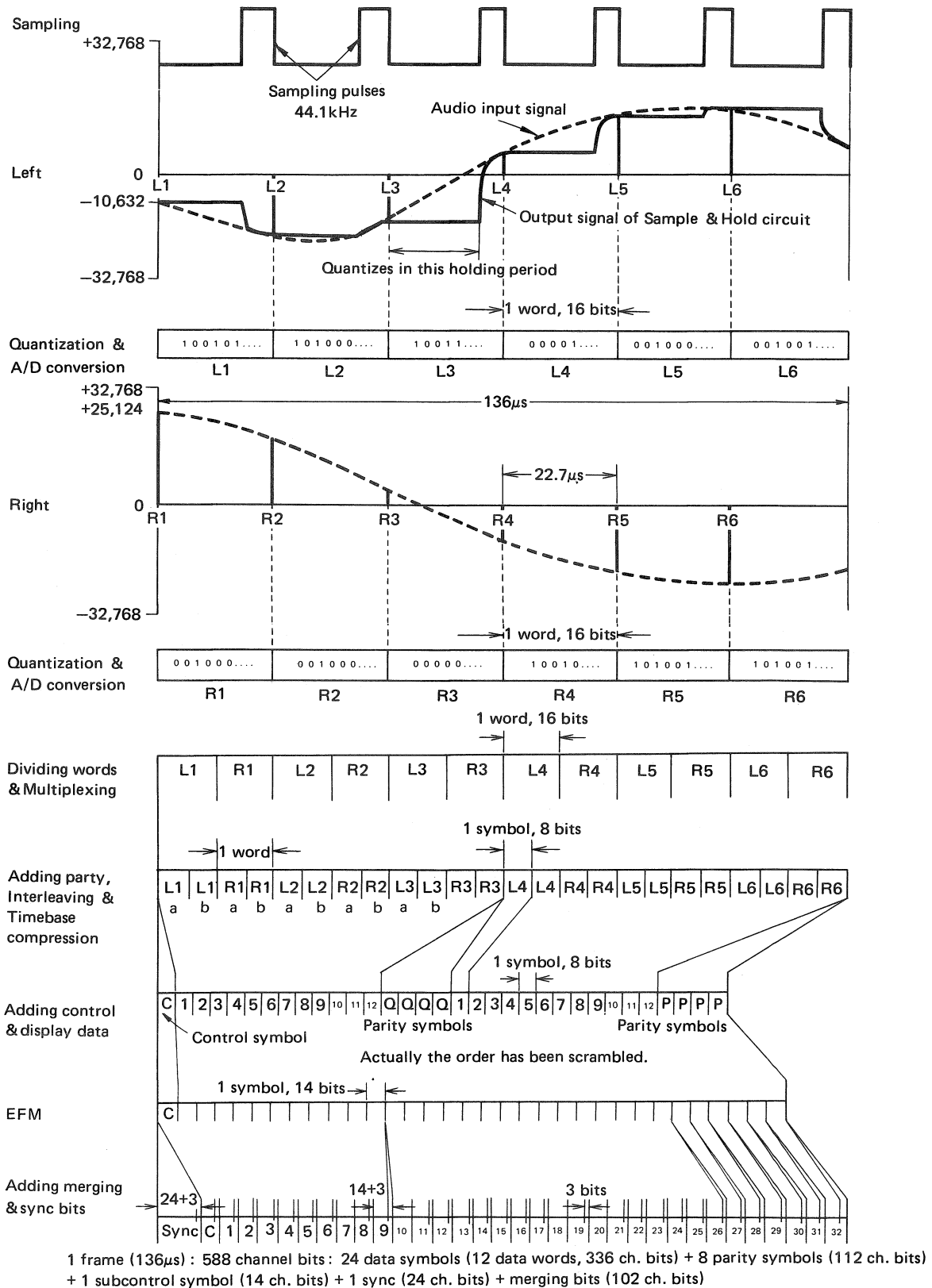


Fig. 6. Encoding Process

2.1 Low-frequency signal filtering (LPF)

The R and L audio signals are amplified sufficiently for processing and are applied to the Low-pass Filters (LPF). These filters pass only the signals of less than 20 kHz thereby avoiding frequency foldover between the audio signal

and the sidebands of the sampling signal, as illustrated below. The foldover causes a noise called "aliasing noise". The 20 kHz is high enough because most of the audio signals have been included in the range from 20 Hz to 20 kHz.

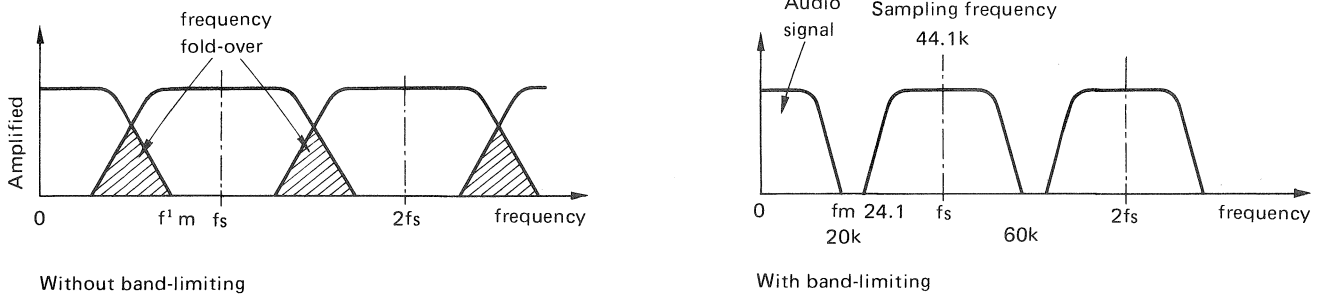
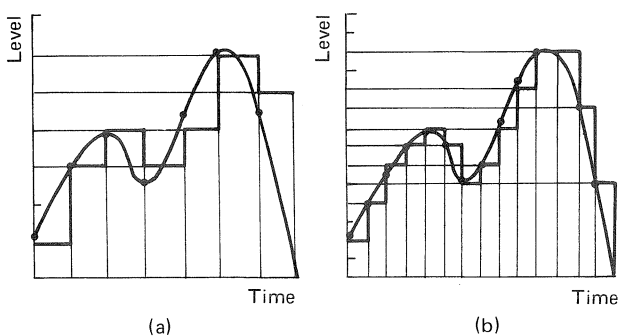


Fig. 7 Frequency Spectrum of Audio Signal and Sampling Frequency

2.2 Sampling

The R and L analog audio signals are sampled at a fixed interval of $22.7 \mu\text{s}$ (44,100 times per second) by sample-and-hold circuits. The signal amplitude is measured as shown in Fig. 8. The higher the sampling frequency, the better. High frequency sampling, however, requires expensive devices. In principle, the sampling frequency of more than twice the maximum frequency of the signal to be sampled is high enough.

The switch in Fig. 8b is operated by sampling pulses of 44.1 kHz. When a pulse closes the switch, the voltage value of the analog input signal is stored in the capacitor. When the pulse disappears, the switch opens, and the value is retained until the switch is closed again. When the next sampling pulse closes the switch, the capacitor stores the new value.



The more the steps and the higher the sampling frequency, the better.

Fig. 8a Sampling and Measuring Audio Signal

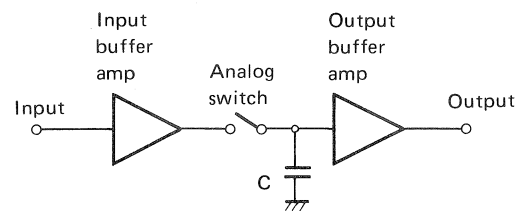


Fig. 8b Sample & Hold Circuit

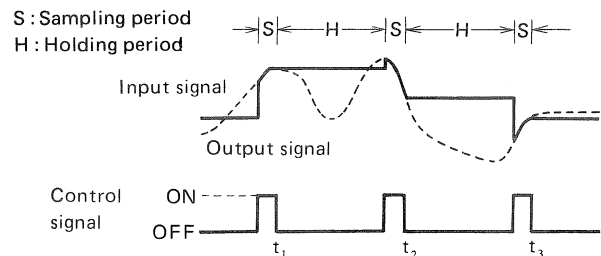


Fig. 8c Sample & Hold Waveform

2.3 Quantization and analog-to-digital (A-D) conversion

Signal voltage amplitude is measured in 65,536 (2^{16}) intervals. The dynamic range (level difference) between 65,536 and 1 is 96.3 dB. This is wide enough for representing music sound.

While stored in the sample and hold circuit, the input signal level is compared with the established range and assigned the 16-bit binary code to which the level most closely approximates. Fig. 9 shows the method of quantization and A-D conversion.

As seen in Fig. 10 the stepped waveform of the quantized signal is distorted. The distortion generates quantization noise in playback. To cancel the noise, a similar signal called "dither" is mixed with the audio signal before quantization.

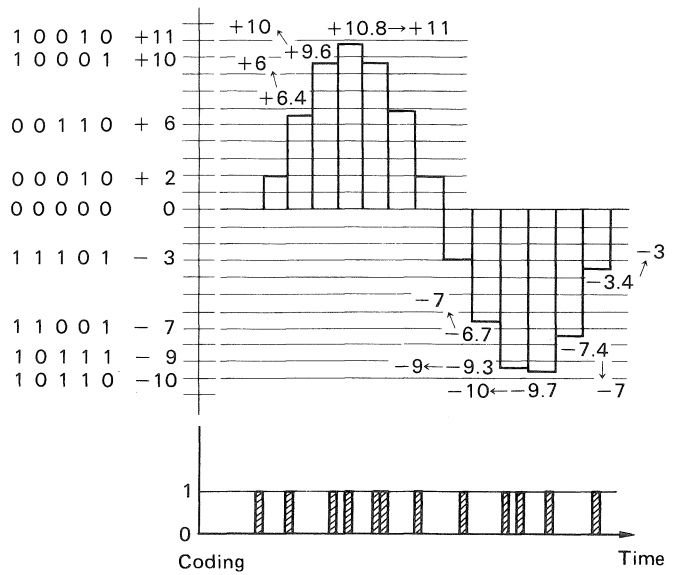


Fig. 9 Quantization and A-D Conversion

2.4 First multiplexing

A multiplexer intermixes and aligns the R and L words one after another in a single data stream. For easier processing in the built-in computer, each 16-bit code is divided into two 8-bit codes. The 16-bit sampled datum is called a "word" and the 8-bit code is called a "symbol".

12 sampled data (6 samples/channel) are grouped into one. This group is called a "frame."

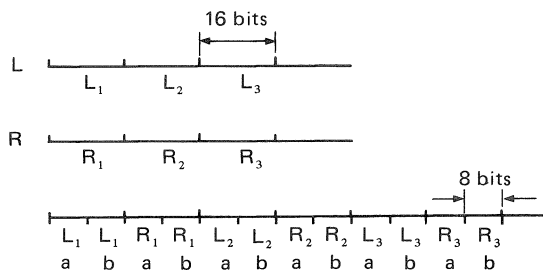


Fig. 11 Aligning and Dividing R and L Words

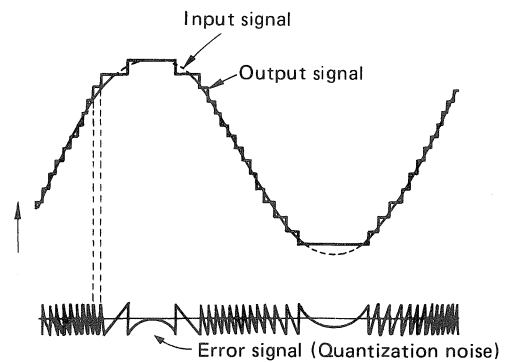


Fig. 10 Quantization Noise

2.5 Inserting check codes

Bit errors are inevitable in the CD system. Most of the errors likely to occur in the process of mastering and mass-production are one or two bit long. Such a short error is called "random error," and occurs an average of a few times per second. A long error, called "burst error," is

generally caused by a scratch or fingerprint and results in all 0's or 1's and error in half of the bits. In the digital system, even a one bit error may result in a different code, causing the production of a completely different waveform from the original one and making a large click noise.

On the other hand, the reproduced signal of the analog system is similar to its original although it may have distortion. CD's error detection and correction are performed by the parity check method.*

*Parity checking method: A digital data checking method in which the total number of binary 1's (or 0's) is always even or always odd. This will be discussed later.

2.5.1 Cross Interleave Reed Solomon Code (CIRC)

CIRC, an effective digital data correcting code, corrects errors by two means: parity check and interleaving. The former corrects random errors and the latter corrects burst errors. The operating principle of CIRC is difficult to understand. Fortunately, however, most of the circuits have been integrated into an IC, and understanding its basic functions is sufficient for performing repair service.

a) Inserting parity bits

Extra bits (parity bits), either 1's or 0's, are inserted between symbols, enabling the decoder to detect and correct errors in the data. This system employs the method of two-fold parity correction with C1 and C2 encoders and three-stage interleaving (scrambling). Fig. 13 shows the encoding process.

b) Interleaving

Burst errors cannot be corrected by the parity check. If, however, the symbols are spread out over a long range when recording, correction becomes possible during playback.

By recording adjoining symbols in places remote from each other, the risk of losing consecutive data can be spread out. Fig. 12 compares correction with and without interleaving. It shows that long errors in interleaved data can be divided into short errors, correctable in the playback process. Interleaving is just like the shuffling of cards in a predetermined order. The order of bits within a symbol is not scrambled throughout the process.

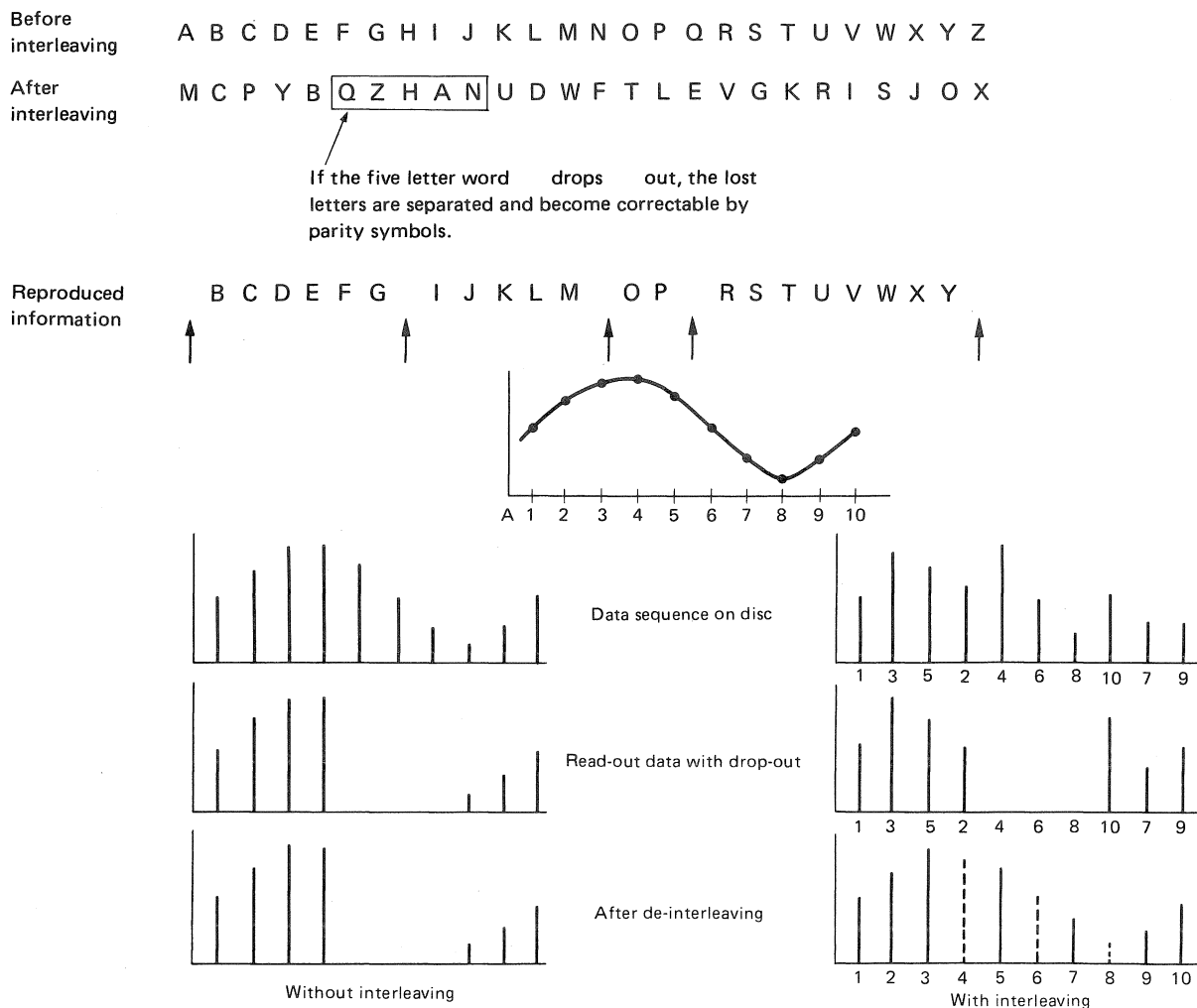


Fig. 12 Sound Processing With and Without Interleaving

2.5.2 Encoding

The encoder processes the 24 symbol data in the following order:

- Even-numbered sample words ($6n$, $6n+2$ and $6n+4$) are delayed by two frames.
- The symbols are scrambled.
- The encoder C2 generates four symbols of Q-parity from the 24 data symbols and inserts the four symbols into the 24 symbols.
- The n th symbol is delayed by $n \times 4$ frames and the 28 symbols including the four Q-parity symbols are spread out over a maximum of 108 frames (27×4).
- C1 generates four P-parity symbols from the 28 symbols including the 4-Q parity symbols, and inserts the P-symbols in the data symbols.
- The even-numbered symbols of the 32 symbols including the Q and P parity symbols are delayed by one frame.
- All of the parity symbols are inverted. If they are not inverted and are dropped out, they may be read as 0's and data may be taken to be correct.

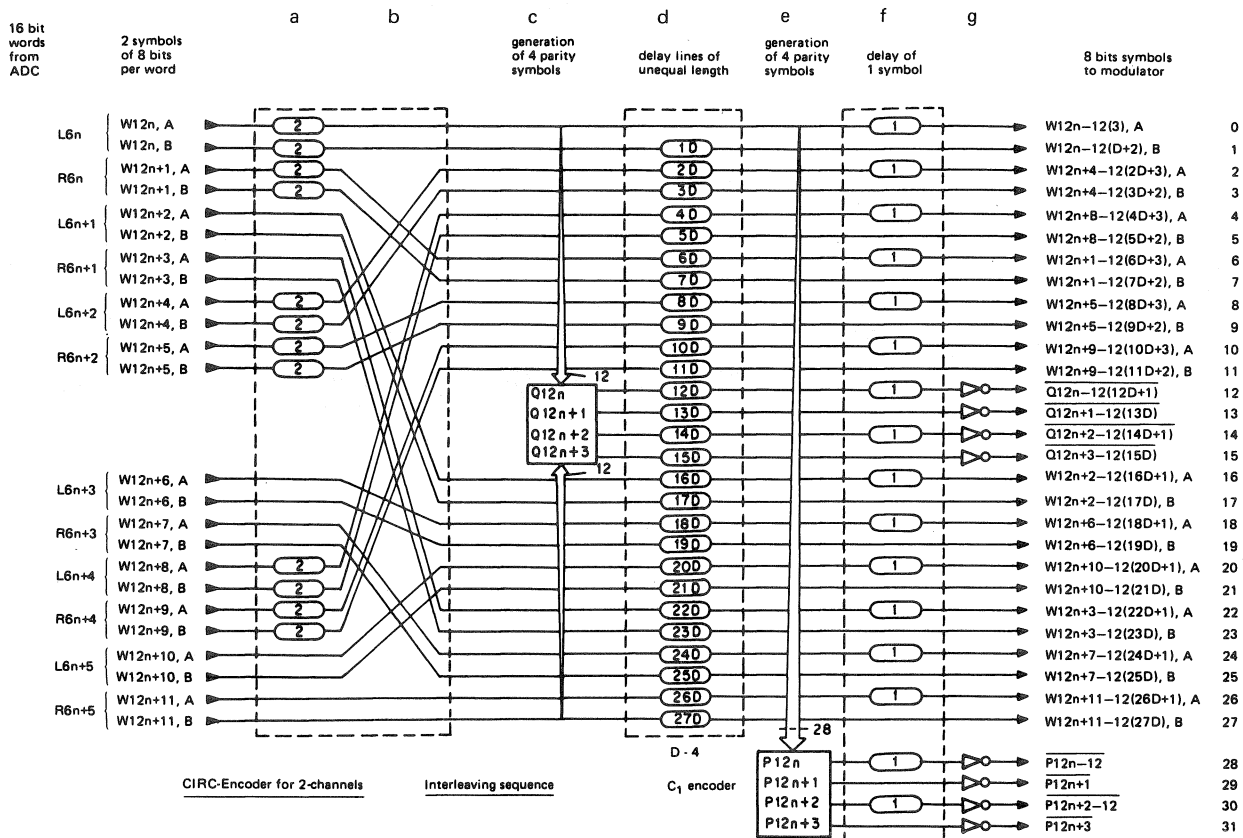


Fig. 13 Encoding Process

2.6 Second multiplexer (inserting control and display or subcodes)

In the LV system, Philips codes of Lead-in, Lead-out, Chapter No., Frame No., etc. are superimposed on the TV V-blanking signal. (TUNING FORK No. 6, p.65). For the same purpose, 8-bit control and display subcodes are inserted at the beginning (next to the frame sync signal discussed later) of each frame which has grown to 32 symbols.

Unlike other data symbols, each bit of the control subcoding symbol or control symbol has a channel name from P to W and carries only a small part of information different from each other.

The data on the subcoding symbol are distributed to 98 frames which is the largest processing unit. The bits on the symbol become meaningful when they are stored in a RAM for 98 frames. It takes 13.3 ms ($98 \times 136 \mu\text{s}$) to store 98 frames in the RAM.

The first two subcoding symbols have particular subcode synchronizing (sync) patterns S0 and S1.

P-channel: While playing, the bit on the P channel is 0 when the pickup is in a recorded area and 1 when it is between music pieces. In the lead-in area it is 0 followed by a start flag ("1" for 2 or 3 seconds).

In the lead-out area, a start flag appears during the last music piece, "0" follows for 2 or 3 seconds, 2 Herz pulses then appear.

Q-channel: The next Q channel has a table of disc contents as shown in Fig. 15. The Q channel has its own sync and check codes.

In the lead-in track a table of contents is recorded. In the table up to 99 music pieces are numbered. A music piece can be subdivided. The minimum length of a piece excluding pausing period is 4 seconds.

Among the 8 channels, the 6 channels from R to W are not being used. The unused channels have been saved for future use.

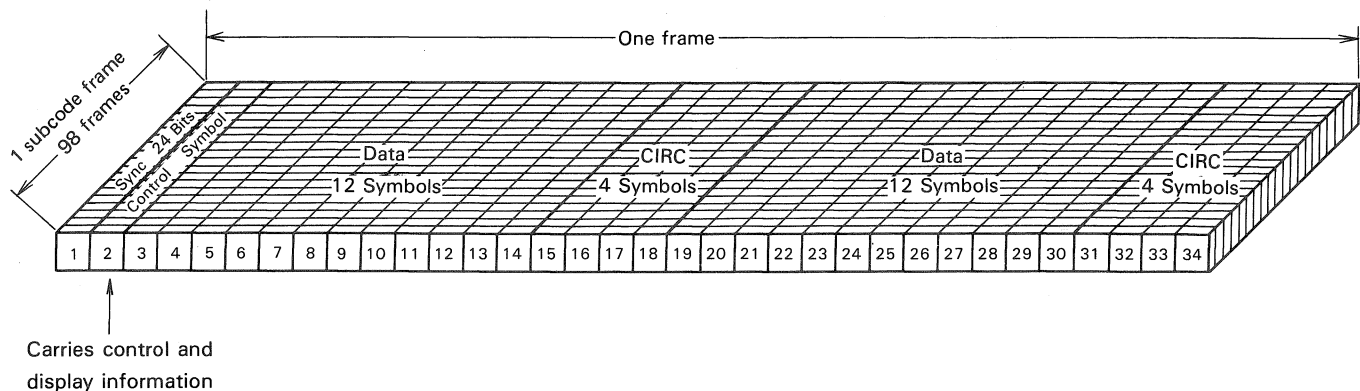
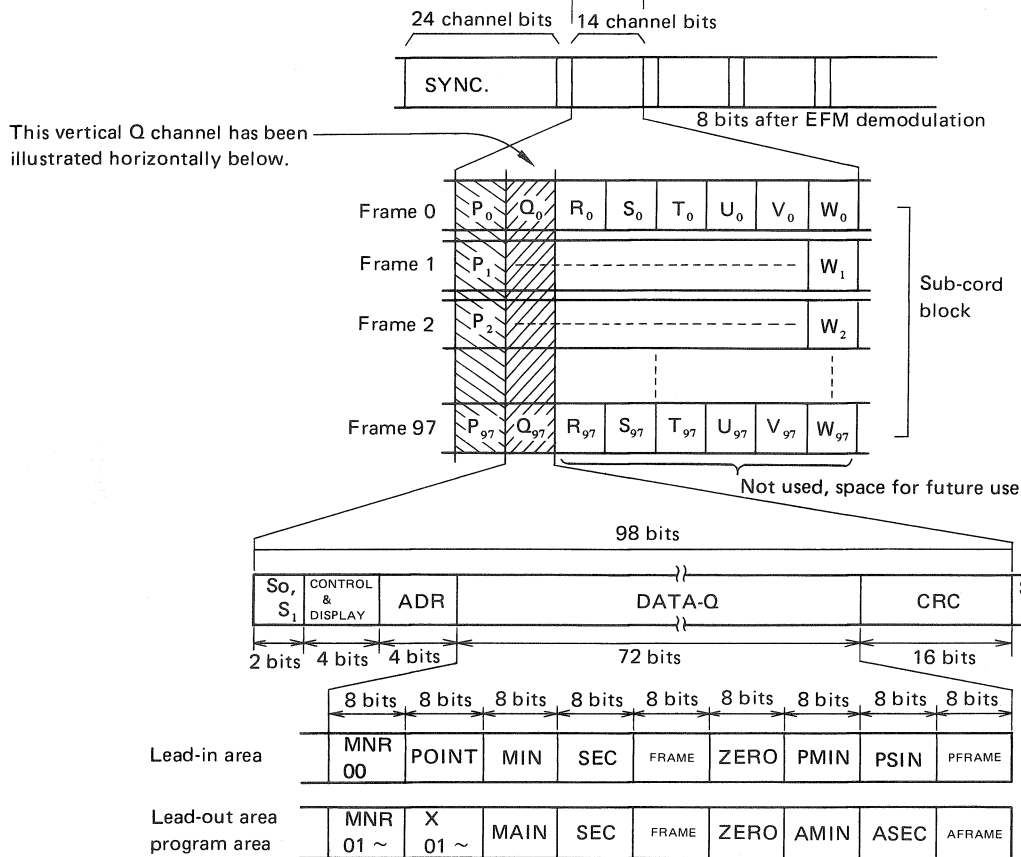
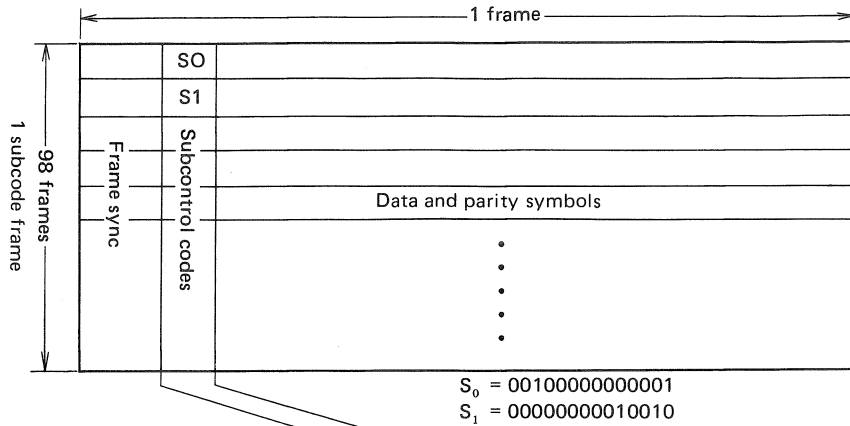


Fig. 14 Frame Composition

1 sample = 1 word = 16 bits = 2 symbols
 1 symbol = 8 bits (14 bits after EFM)
 1 frame = 1 sync code + 1 control & display symbol
 + 24 data symbols + 8 parity symbols
 Frame rate = 7.35k frames/sec
 Subcode bit rate = 58.8k bits/sec



P channel

Within music: 0
Between music: 1
Lead-in area: 0 → A start flag ("1" for 2 or 3 sec.)
Lead-out area: A start flag → "0" for 2 or 3 sec. → "0" and "1" at 2Hz

0
1
0 → A start flag ("1" for 2 or 3 sec.)
A start flag → "0" for 2 or 3 sec. → "0" and "1" at 2Hz

Q channel

S_0, S_1 : Sync code
Control: 2 or 4 channel/15 or 50 μ sec de-emphasis
Address: Mode 1: Address
Mode 2: Disc catalog number
Mode 3: Copyright, recorded date & serial No.
CRC: Cyclic redundancy check code (parity)

MNR: Music number —

Lead-in (TOC): 00
Music number: 01-99
Lead-out: AA
Start/End: 00
Index number 01-99 (subdivision number)
Table of content (TOC)
Elapsed time per music piece
All zero (for future use)
Absolute time
Starting point of the music number

X: Index to MNR —
(within a music piece)

POINT:

MIN, SEC & FRAME:

ZERO:

AMIN, ASEC & AFRAME:

PMIN PSFC & FRAME:

Fig. 15 Control and Display Codes

2.7 Eight-to-fourteen modulation (EFM)

At this point, 8-bit codes are converted into 14-bit codes, as shown in Fig. 17. The signal level is shifted when a 1 appears. For high density recording and easy signal pick-up, it is better to narrow the frequency spectrum by reducing the length variation of pits and flats. For high accuracy in reading codes, similar bit patterns should be avoided. To meet these requirements, the following conditions have been made:

- To make the high end of the frequency spectrum low, the shortest pit should be 3 bits long or there must always be at least two 0's between successive 1's. The greater the minimum length between transitions (T_{min}), the better. When pits or flats are very close to each other, as shown in Fig. 16, the beam cannot read the edge of the pits correctly.
- To make the low end of the frequency spectrum high, the longest pit should be 11 bits long or there must be no more than 10 consecutive 0's in any part of the string of codes. The shorter the maximum length between transitions (T_{max}), the more exact the timing of the player. Furthermore, if the flats are too long, the laser beam cannot search and track the string of pits.
- To avoid mistaking one code for another when reading, the minimum code distance* should be as great as possible, or the bit patterns should be as different as possible from each other. If 00001001 and 10001001 are employed, a single error in the MSB or the left-most bit would make another code. The distance between these codes is 1 bit.

*Minimum code distance: The smallest number of bit errors which would convert one code to another in a code system. This is called "hamming distance."

Among the 256 combinations of 8-bit codes, there are many which do not satisfy the above constraints. 14-bit codes, however, have 16,384 (2^{14}) combinations. This is sufficient to represent 256 kinds of data even when unsatisfactory combinations are eliminated. 256 combinations out of the 16,384 codes are selected to represent the 8-bit data in a one-to-one relationship between the two types of codes. There is no direct relation between the 16-bit codes and 8-bit codes. The relation is just like that of the alphabetical characters to the Morse codes. The conversion table is stored in a Read Only Memory (ROM).

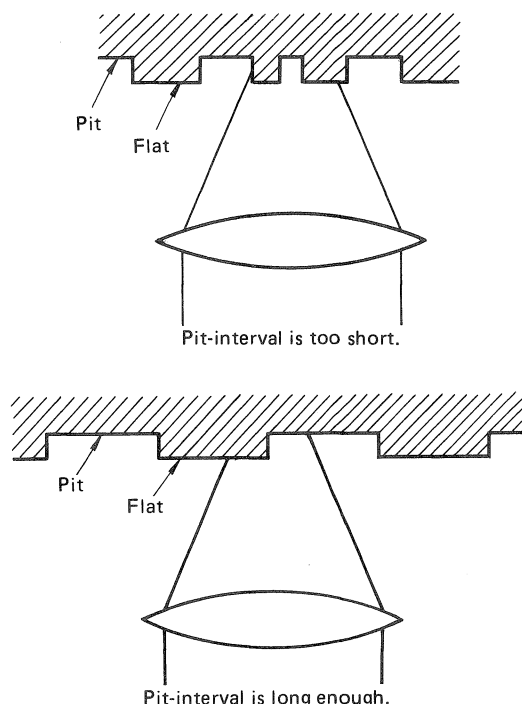


Fig. 16 Inter-pits Interference

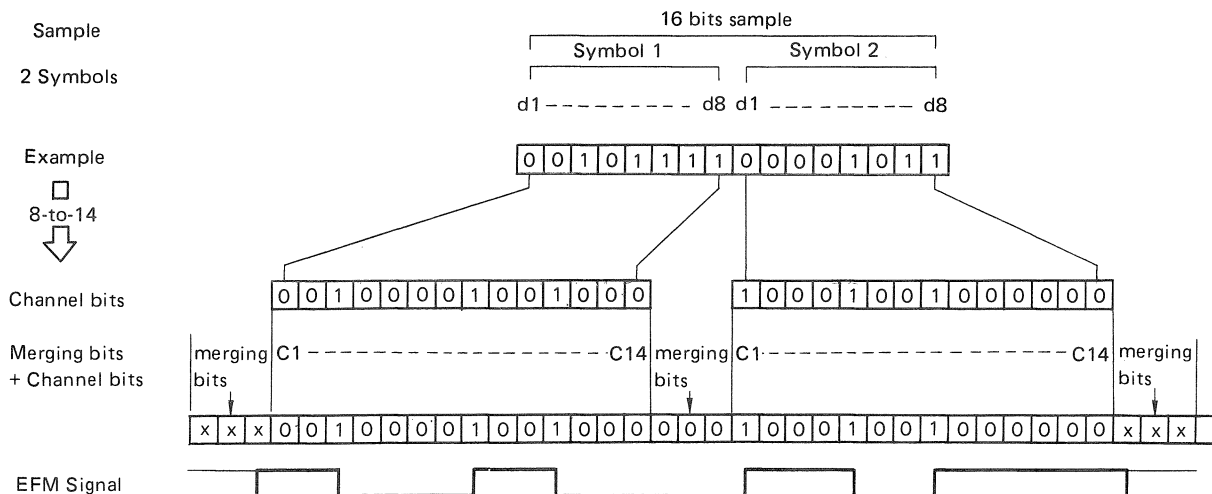


Fig. 17 EFM

When being EFMEd, the signal wave is converted from NRZ to NRZI* to make pit (flat) length long and avoid inter-pits interference.

*NRZ and NRZI: Among many digital modulation systems, the CD system employs the following two systems.
 NRZ: (Non Return to Zero): The signal level becomes H at 1 and L at 0. This method is employed for processing digital data.
 NRZI (Non Return to Zero Inverted): The signal inverts at the center of 1. This is employed in cutting the disc because it makes longer pits than NRZ does as shown in Fig. 18.

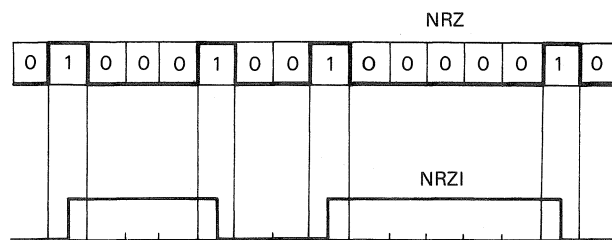


Fig. 18 NRZ and NRZI waveforms

2.8 Inserting 3 merging bits (symbol couplers)

Three merging bits are inserted between symbols as a coupler. Their functions are:

- a) Satisfying the requirements of Tmax and Tmin: When two symbols are connected, the Tmin and Tmax requirements may not be satisfied at the coupled point. When the adjoining bits of adjoining symbols are both 1's, three merging bits become 0, and when the adjoining bits are both 0's among 10 or more consecutive 0's, one of the three merging bits becomes 1 in order to avoid having eleven 0's in succession.
- b) Suppressing low frequency component: If the above requirements are satisfied and merging bits can take either state, the processor selects either 0 or 1 to suppress the component contained in the EFM signal. For the suppression, the digital sum value* should be minimized, or the average duty ratio* for a long period should be 50%. If long (-1's) pits continue and the average level becomes lower than 1/2 of pulse peak, one of the merging bits becomes 1, thereby shift-

ing the level and making a flat (+1's) period. Refer to Fig. 19.

*Digital Sum Value (DSV): In regard to digital square waves, the sum value in a long period by assigning +1 and -1 to the high level and low level respectively. (Fig. 19)
 *Duty ratio: In a pulse system, the ratio of average to peak power. Refer to Fig. 20.

- c) Synchronizing the data stream with the reference clock signal: A 4.3218 MHz clock is required to synchronize the data stream with the player's operation. The CD signal itself does not have such a high frequency. The nine waves, however, have the clock signal component as shown in Fig. 2. Pulse edges are extracted from the data stream and compared with the phase of the player's clock to maintain exact timing. The more pulses, the better for the synchronization.

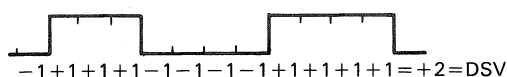


Fig. 19 Digital Sum Value

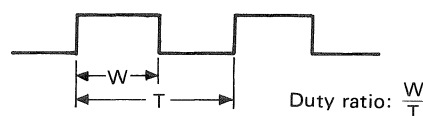


Fig. 20 Duty Ratio

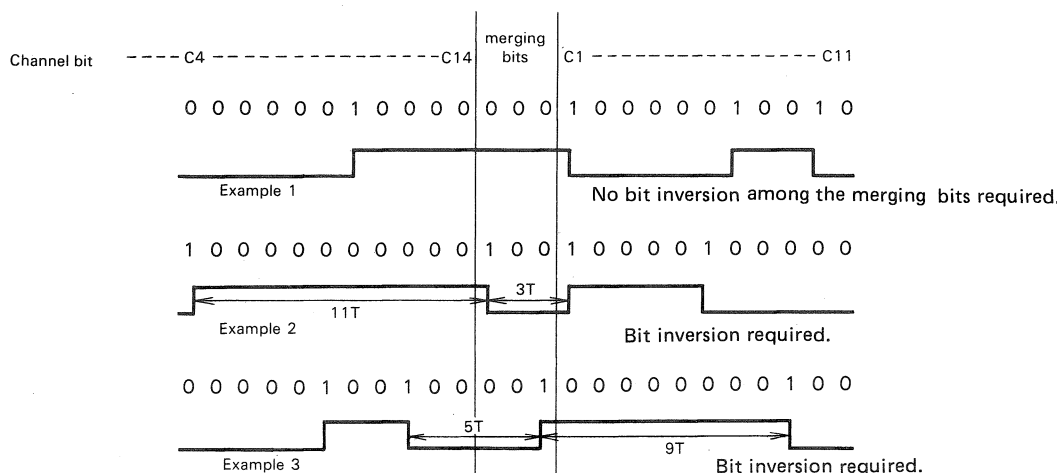


Fig. 21 Merging bits

In case low level continues, one of the merging bits inverts the level.

2.9 Inserting frame synchronizing (sync) signal

TV and LV signals use Horizontal and Vertical syncs to give receivers and monitors an accurate scanning timing. The CD also uses frame sync signals to time its operation. A unique sync pattern is placed at the head of each frame. If a frame sync pattern is dropped out or deformed

when decoding, the frame starting point will be undetectable, errors will occur continuously and subsequent data will become meaningless. This phenomenon is called "error propagation."

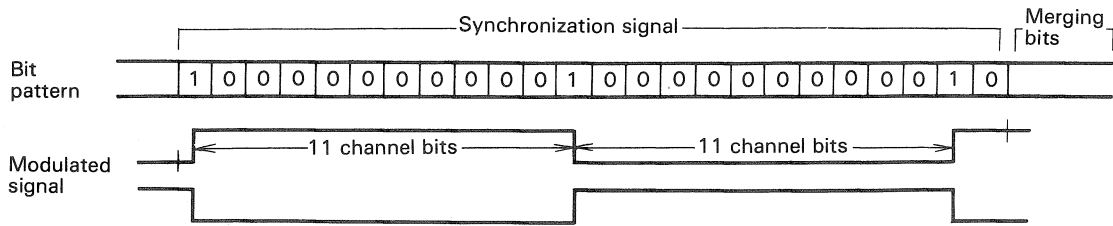


Fig. 22 Sync Patterns

Now a frame has been completed. Fig. 23 illustrates one full frame of complete composite EFM signal for the 12 samples.

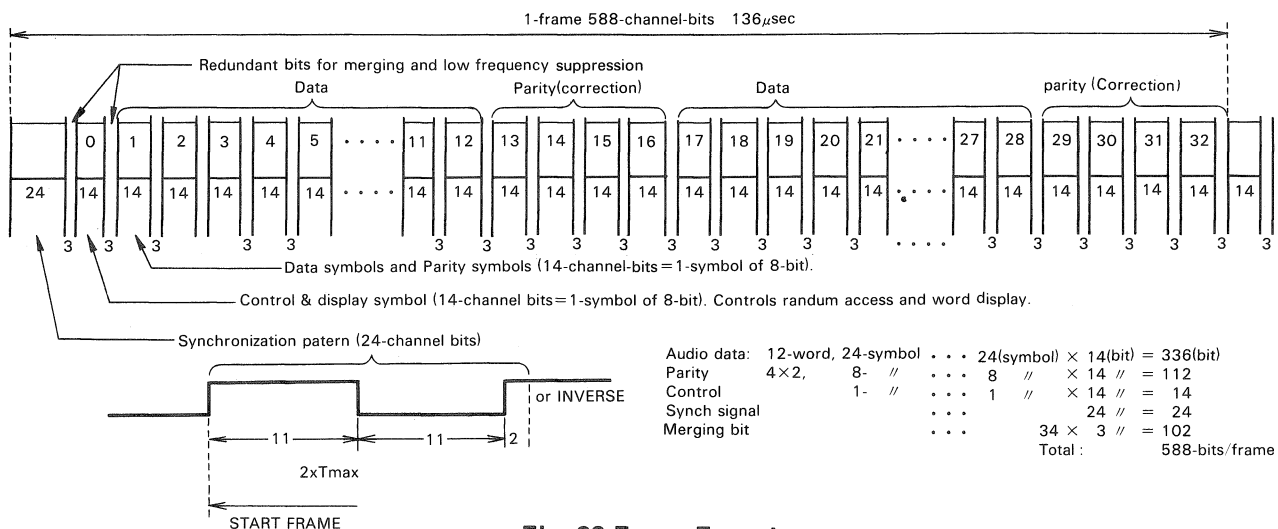


Fig. 23 Frame Format

1 sample: 1 word: 16 bits, 2 symbols
 1 data or parity symbol: 14 bits (8 bits before EFM)
 1 subcoding symbol: 14 bits (Note that meaningful information is on the accumulated 98 frames.)
 1 sync signal: 24 channel bits
 1 frame: 6 samples/channel: 12 data words
 1 frame = 1 sync (24 bits) + 1 control symbol (14 bits) + 24 data symbols (336 bits) + 8 parity symbols (112 bits) + 34 sets of merging bits (102 bits) = 588 channel bits

Sample rate: 44.1k samples/sec/channel
 Data bit rate: 1.4M bits/sec (5 billion bits/H)
 Frame rate: 7.35k frames/sec (75 subcode-frames/sec)
 Control bit rate: 58.8k bits/sec
 Transfer rate: 2.03M bits/sec before EFM
 Bit rate (clock frequency): 4.3218M bits/sec
 Channel bit: The final bit after processing is completed.

2.10 Optical cutting

The composite signal is applied to the laser beam modulator on the master disc cutter to turn the beam on and off in the same way as that of the LV system.

3. Playback

The playback process is essentially the reverse of mastering. Fig. 24 shows a block diagram of the player.

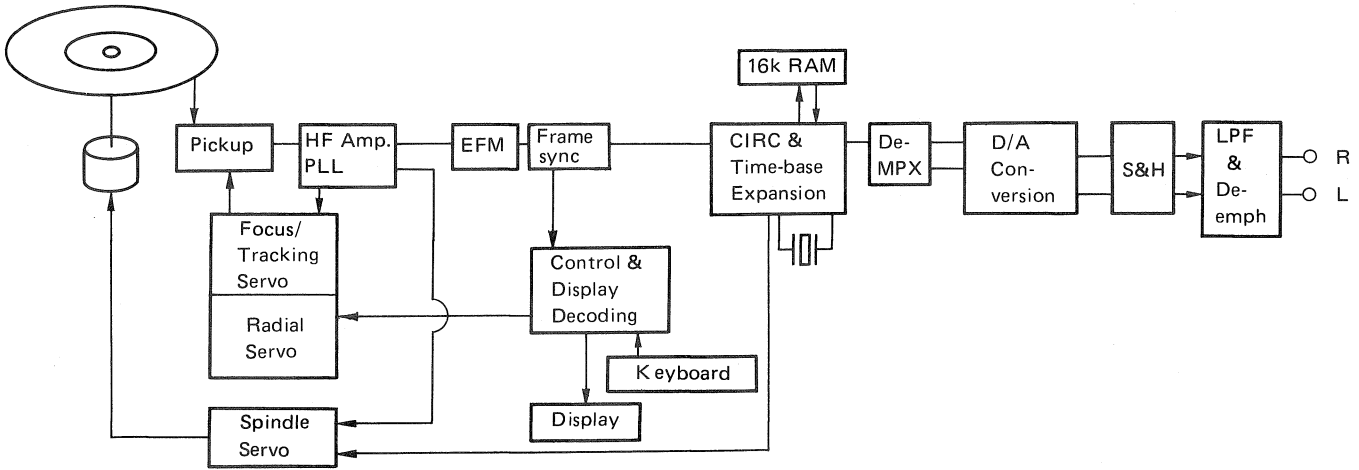


Fig. 24 Block Diagram of the Player

3.1 Retrieving HF signal

The bright and dim light reflected from the disc is transduced to electric signal by photodiodes. In the HF amp, the high frequency signal is filtered and amplified by 14 dB. Fig. 25 shows the waveform of the transduced signal.

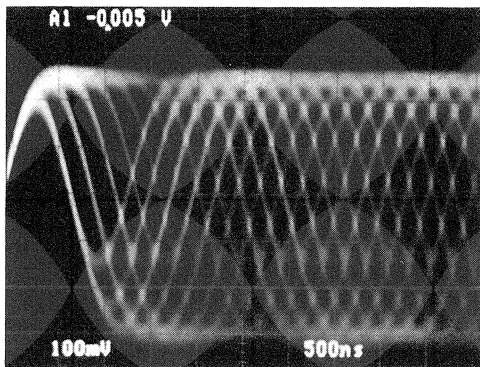


Fig. 25 High Frequency Signal

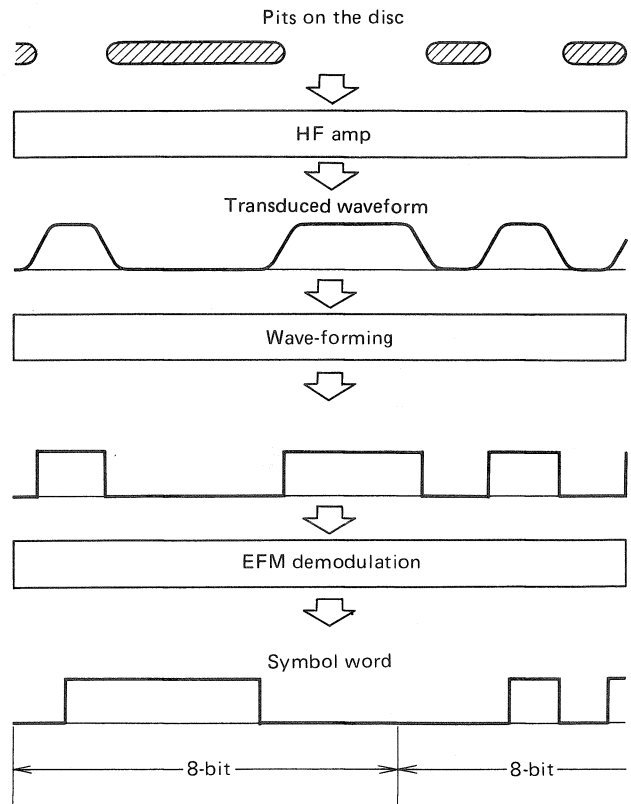


Fig. 26 Reproducing Squarewaves

3.2 EFM pulse wave forming

The slope of these waves is not as sharp as pulse waves. The sharper the slope of the waves, the better for detecting the signal level. In other words, the thinner and taller the diamonds in the pattern of Fig. 27, the better. Another problem is that, when cutting, all the pits become longer or shorter (depending upon mastering conditions) than the actual pulse-width of the EFM signal to be recorded, caus-

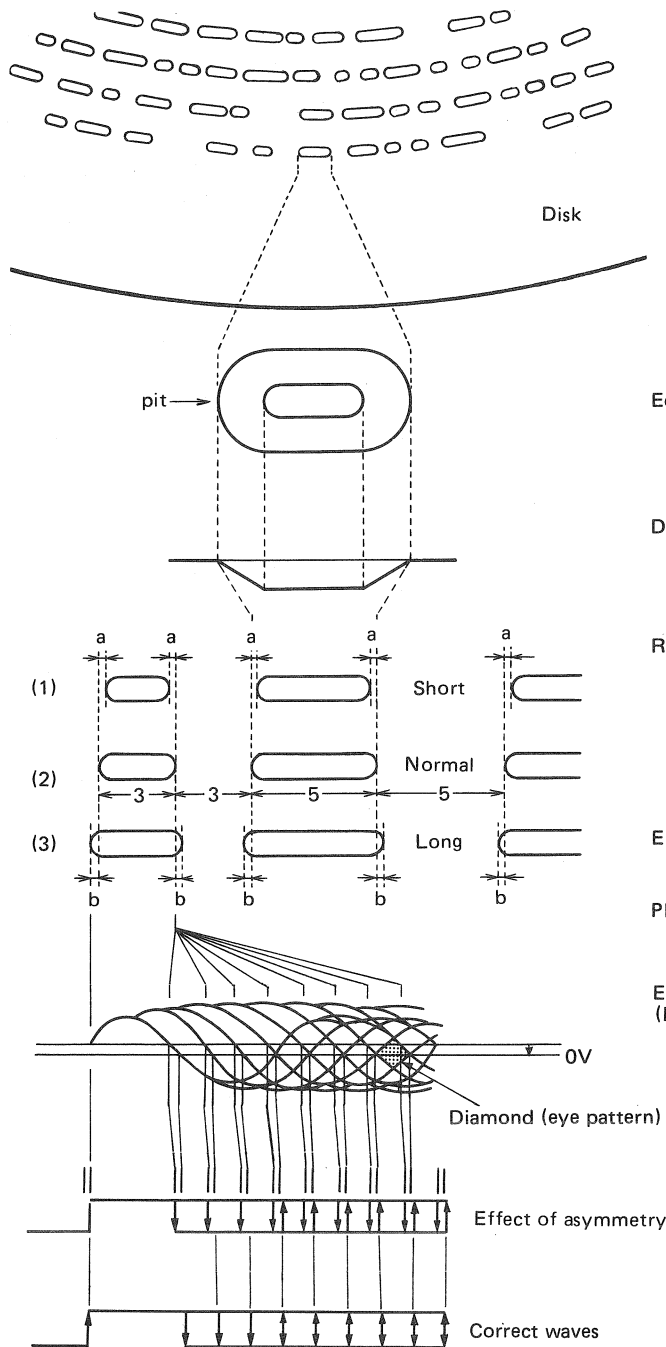


Fig. 27 Automatic Threshold Control Shifts the Threshold Level to the Center of the Wave

ing the RF signal to become asymmetrical to the 0V level. The threshold level is adjusted and DC offset is eliminated by an Automatic Threshold Control in order to achieve the correct pulse width. As shown in Fig. 28, the pulse generator has a slope-sensing window of one cycle period (1T) for correctly reading a signal which has some jitter or time-base error.

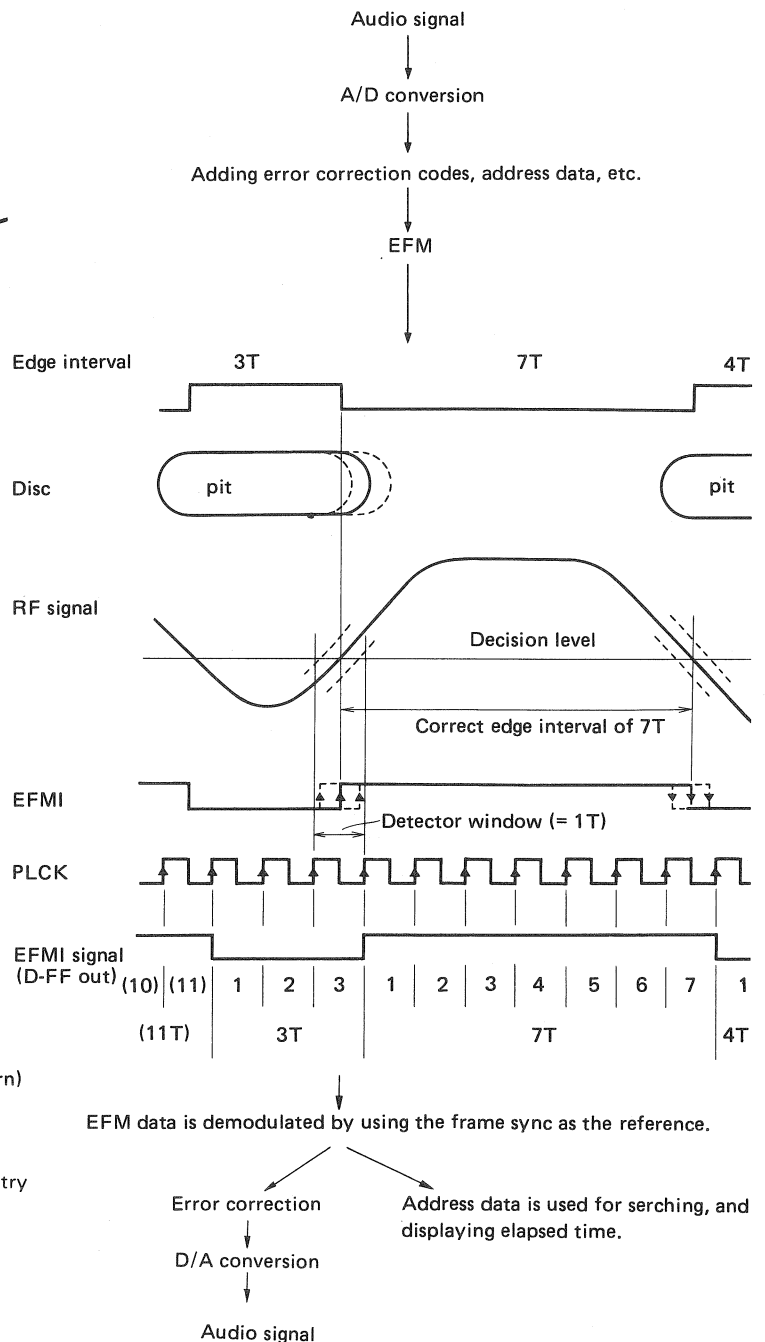


Fig. 28 Slope-sensing Window for Time-base Error Absorption

3.3 Extracting pulse edges

Pulse edges are extracted from the data signal and applied to the Phase Lock Loop (PLL) servo circuit. The PLL circuit compares the pulse phase with that of the reference signal generated in the player and controls the motor speed. As the pickup moves outward, the diameter of the track and the speed of the pits relative to the pickup increase. A negative servo signal is then introduced, gradually slowing the motor speed from 500 r.p.m. to 200 r.p.m. in order to maintain a constant linear velocity.

Frame sync is used for controlling the motor. 11 clock pulses should be in a sync pulse period. If the sync pulse is longer than 11 clock waves, the motor speed is accelerated. Refer to Fig. 22.

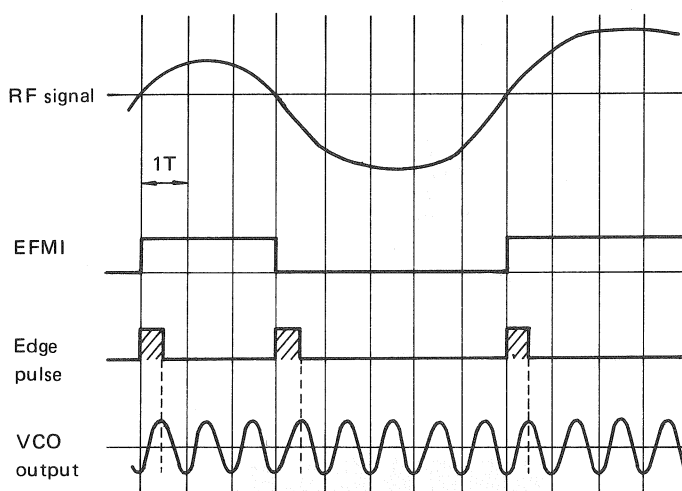


Fig. 29 Extracting Pulse Edges

3.4 Demodulating EFM signal

In the EFM demodulator, EFM codes are demodulated. 14-bit symbols are converted into 8-bit symbols in accordance with the built-in conversion table and are fed to the CIRC circuit.

3.5 Frame synchronizing

The frame sync gives the decoder a timing to start processing each frame data. Refer to 2.9.

3.6 Control and display

Subcontrol symbols are separated and decoded in the Control Display circuit. Parity check is performed separate from sound information.

The table of contents and other information on the Q-channel are memorized in a RAM to prepare for time and index number display, random access, repeat play and programmed play.

3.7 CIRC error detection and correction

The decoder detects and corrects errors as follows (Fig. 30):

- a) The odd-numbered symbols are delayed by one frame.
- b) All parity symbols are inverted.
- c) In the decoder C1, errors are detected and corrected by the P-parity symbols. It detects errors of three symbols and corrects those of two symbols. One symbol errors are corrected without setting error pointers (flags for locating errors). If two symbol errors are detected, they are corrected and pointers are set to 1, because of the possibility of miscorrection. If errors are detected in three or more symbols, pointers are set to 1 for all symbols (including correct symbols) in the frame, and no correction is performed. This indicates that there is a possibility of error in all of the symbols, excluding the four P-parity symbols. P-parity symbols disappear after used.
- d) The output of C1 is delayed for a predetermined number of frames. The delay time varies depending upon the symbol involved, and is symmetrical to that of the encoder.
- e) In C2, the 24 data symbols are corrected by the four Q parity symbols. C2 corrects up to three errors. C2 reads the C1 pointers and estimates the result of its correction. When the probability of miscorrection is low, correction are performed. If the probability of miscorrection is high, C2 sets pointers after correcting the errors. If the error is long, C2 sets pointers without performing correction.
- f) De-scrambling is performed in the reversed way to encoding.
- g) Those words which were not delayed by 2 frames at the beginning of encoding are delayed by 2 frames here. At this point, the words have been rearranged in their original order.
- h) The words are output in series, beginning with the LSB of the 0th symbol.
Throughout the interleaving and de-interleaving, each symbol is delayed by 111 frames.

The CIRC corrects burst errors up to 14 frames or about 450 symbols for the period of 1.9 millisecond or the length of 2.55 millimeters. The decoder IC checks the quantity and location of C2's error pointers, and determines whether to output the data directly, to interpolate it or to mute the sound.

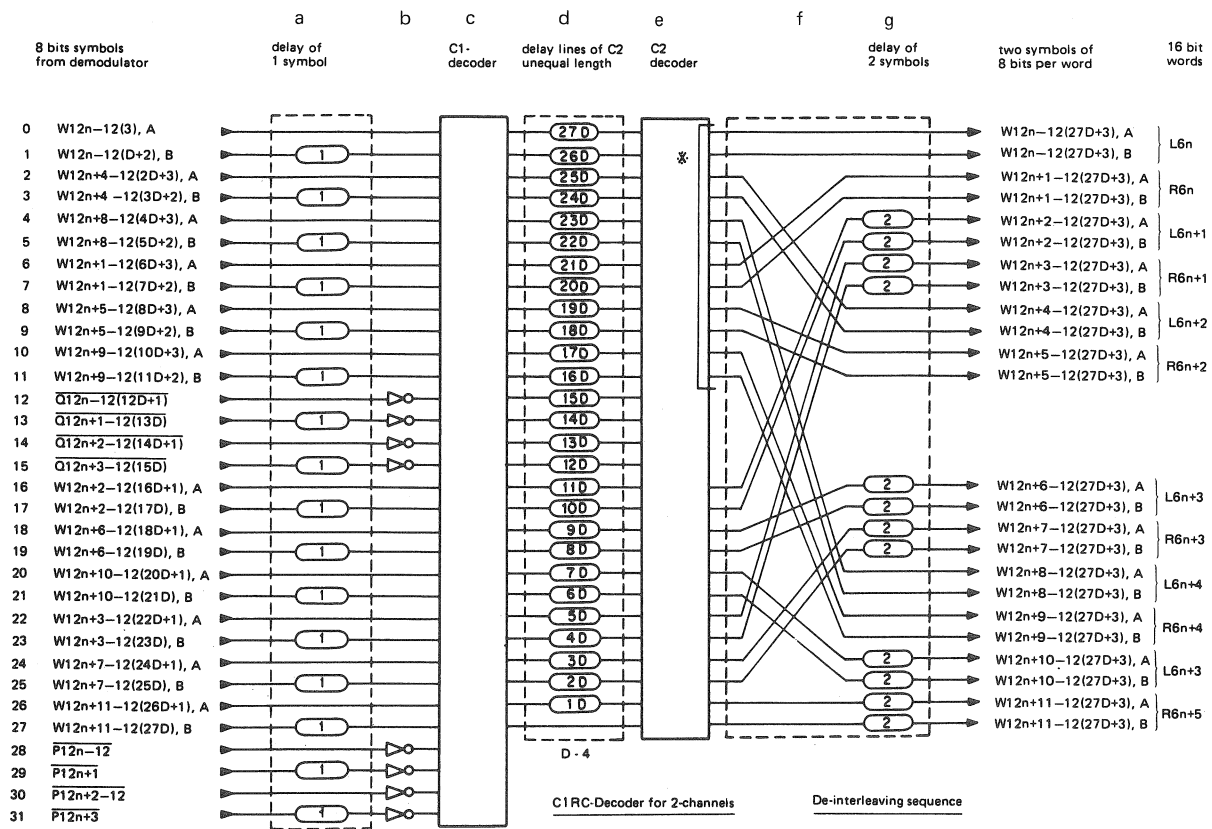


Fig. 30 Decoding Process

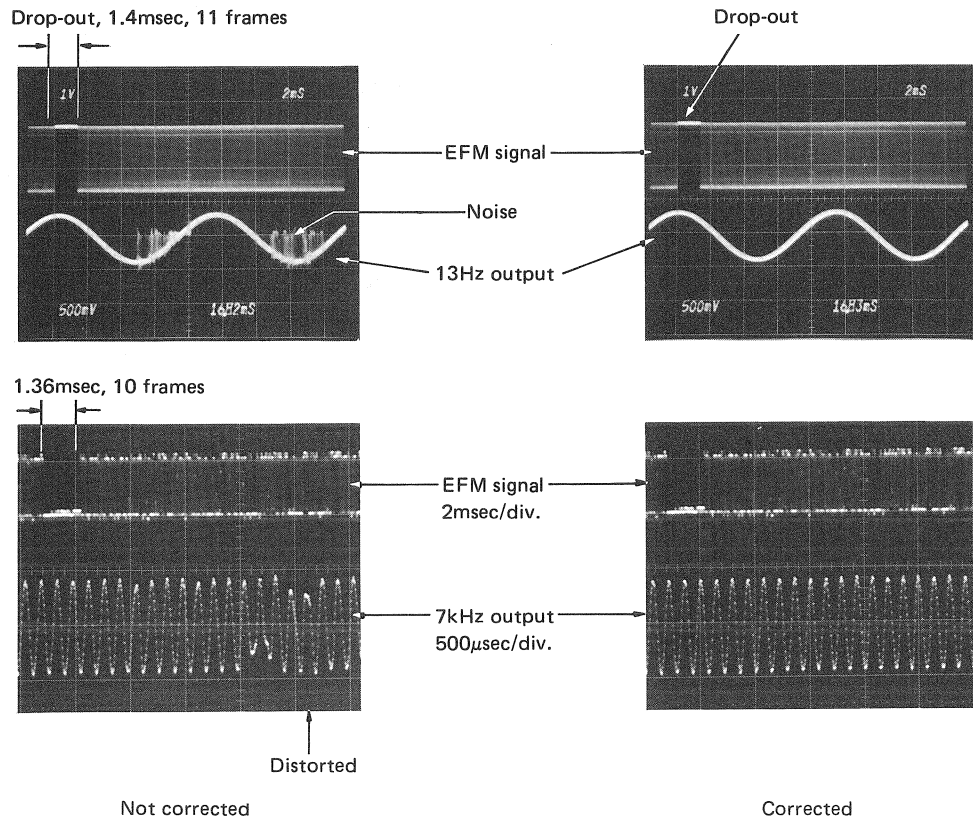


Fig. 31a Drop-out Correction

3.8 Interpolating

Uncorrectable drop-outs for the length up to 48 frames or 8.72 millimeters are interpolated. When the correction at the MSB of a high level sample is unreliable, interpolation is performed to prevent a loud click noise. If the drop-out is longer than 48 frames, the sound is muted.

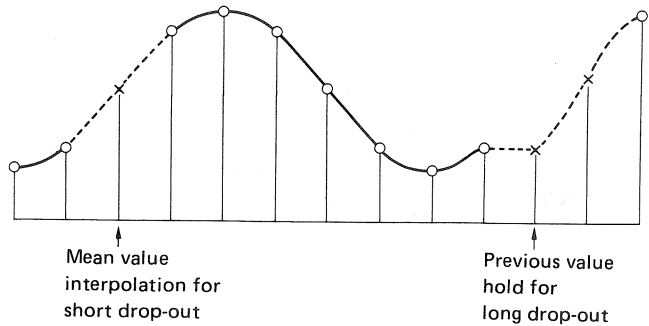


Fig. 31b Interpolation

3.9 Speed control with RAM

Being controlled by a quartz oscillator and independent from the PLL circuit, the RAM connected to the CIRC block for correcting and rearranging the string of data works as a reservoir and tangential servo controller, or jitter absorber. The RAM pools received data and outputs such data with the accuracy of quartz oscillation. The CD's wow/flutter, therefore, also has such accuracy. The RAM-control IC generates a speed control signal for the spindle motor. If the data quantity pooled in the RAM's rear room exceeds a certain level, a negative DC signal is generated and applied to the motor to slow it down.

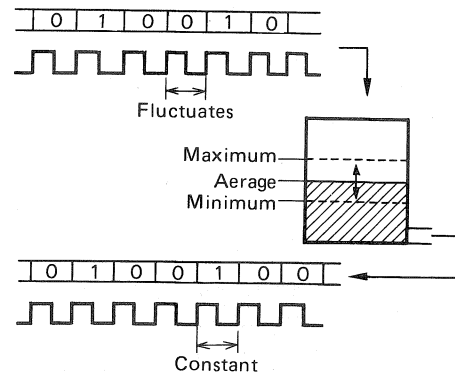


Fig. 32 RAM Reservoir

3.10 Demultiplexing

At this point, the R and L channel data are separated. The complete 16-bit words are reproduced by connecting two symbols.

3.11 D-A Conversion

The 16-bit codes are pulse-amplitude-demodulated and are converted into analog.

3.12 Sample-and-hold

The output of D-A converter is still pulsive. The sample-and-hold circuits convert the R and L pulses to stair waves.

3.13 Low-frequency signal filtering

The edges of the stair waves are smoothed.

3.14 De-emphasizing

If the audio signals were pre-emphasized when recording, they are de-emphasized here and recover their original waveforms.

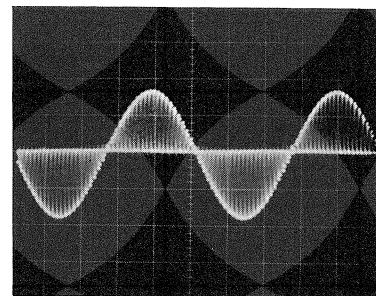


Fig. 33 Output of Sample and Hold Circuit

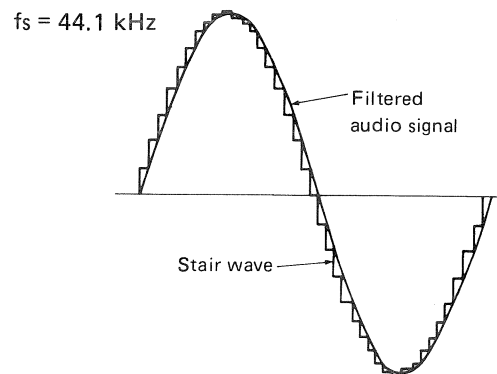


Fig. 34 Stair wave to Audio Signal

4. Expanding Functions

Laser Digital Disc (LDD), our new type of LV disc, has digital sound information, in addition to conventional analog information. There is vacant space below 2 MHz in the NTSC type LV frequency spectrum. The 0-2 MHz CD signal is inserted in this space and adds high quality sound to the fine pictures.

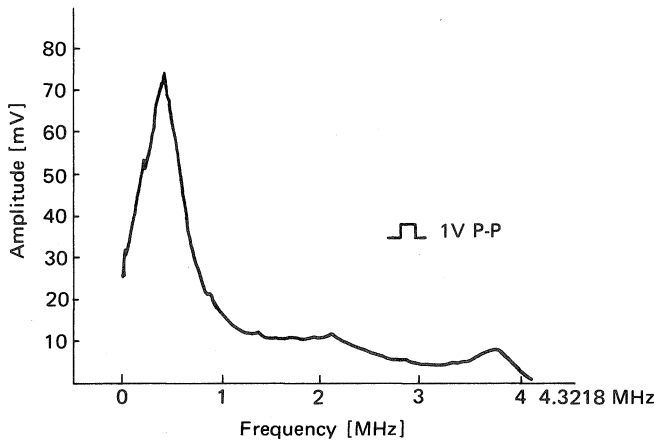


Fig. 35 Actually Measured Frequency Spectrum of CD's EFM Signal

5. Supplement — Simplified Examples of Error Detection and Correction

There are many kinds in the correcting methods of binary codes. Here, we will discuss simplified methods including that of CD System. When transmitting or recording digital signals, binary codes consisting of 0's and 1's are used. In the even parity checking method, the total quantity of 1's in a binary code is always made even by adding an extra bit, 0 or 1, called parity bit to the data code.

Example 1: Crossword Bit Error Detection and Correction

Information word	Binary codes
A :	1 0 1
B :	1 1 1

Assume that the above two 3-bit information words are encoded and decoded.

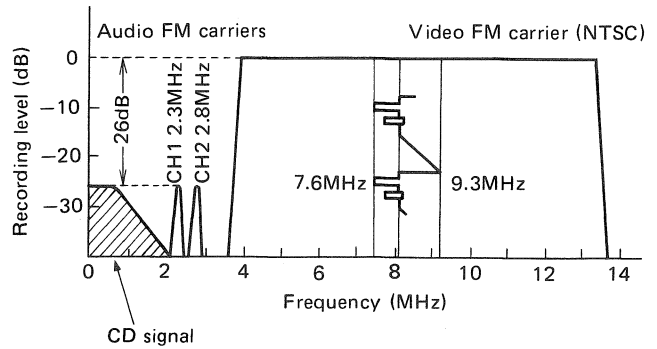


Fig. 36 Spectrum of LDD Signal Containing CD Signal

On the other hand, in the near future, still pictures will be recorded in the CD. Picture information can be recorded in the vacant channel space from R to W in the subcontrol symbol shown in Fig. 15.

Our new LD-CD compatible player CLD-900 is capable of playing both LV and CD discs.

a) Encoding

Data bits are totaled by Modulo-2 addition* horizontally and vertically on respective rows and columns. If the total is an even number, the parity bit is assigned the value "0", if it is odd, the bit is assigned the value "1". The horizontal parities P and vertical parities Q in Fig. 37 are recorded together with information words.

Information Word	MSB (1)	2SB (2)	LSB* (3)	Horizontal Parity PP
A	1	0	1	0
B	1	1	1	1
Vertical Parity PQ	0	1	0	(1)
	Q1	Q2	Q3	

Recorded data

$$\begin{aligned}
 PA &= 1 \oplus 0 \oplus 1 = 0 \\
 PB &= 1 \oplus 1 \oplus 1 = 1 \\
 Q1 &= 1 \oplus 1 = 0 \\
 Q2 &= 0 \oplus 1 = 1 \\
 Q3 &= 1 \oplus 1 = 0 \\
 P &= PA \oplus PB = 0 \oplus 1 = 1 \\
 Q &= Q1 \oplus Q2 \oplus Q3 = 0 \oplus 1 \oplus 0 = 1 \\
 P &= Q = 1
 \end{aligned}$$

* : Symbol of Modulo-2 addition*
Horizontal sum
Vertical sum

Fig. 37 Generating Parity Bits

***Modulo-2 addition**

The symbol of \oplus (modulo-2 addition) does not mean simple "plus" but one-by-one bit addition clearing the result whenever the accumulated number becomes 2. It is processed by 2-input exclusive-OR gates. A 2-input exclusive OR-gate outputs 1 only when its binary inputs are different each other as shown in Table 1.

Inputs		Output
0	0	0
0	1	1
1	0	1
1	1	0

Table 2 Truth Table of an Exclusive OR

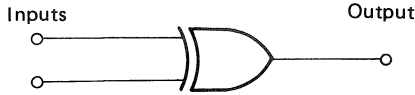
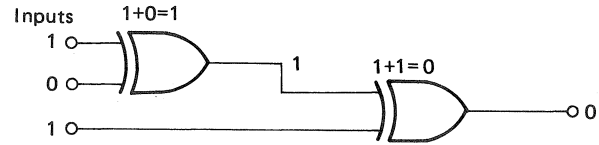


Fig. 38 Symbol of a 2-input Exclusive-OR Gate

The output becomes 1 only when the total of 1's is odd. Throughout the process the bits are not calculated arithmetically but as follows:

$$1 + 1 = 0 \text{ and } 0 + 1 = 1 = 0 - 1$$

When the input code is 101;



$$1 + 0 + 1 = \dots\dots\dots 0$$

Fig. 39 Cascode Exclusive-OR Circuit for 3-bit Modulo-2 Addition

b) Error detection

When decoding, the 1's including the parity bit are totaled both horizontally and vertically in the same way as generating parities. These values are called "syndromes." If there is no error, all syndrome bits are 0.

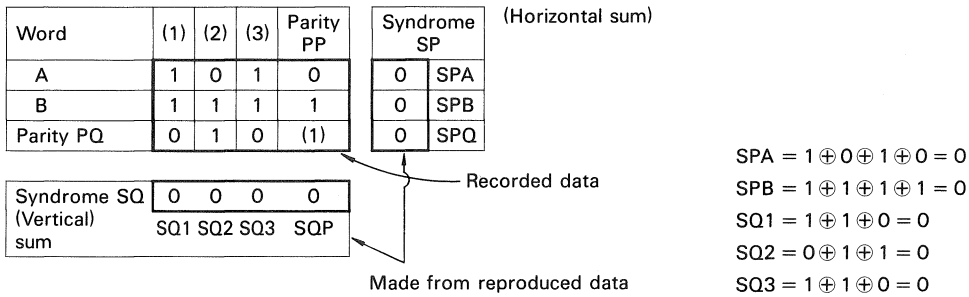


Fig. 40 Syndromes When No Error Occurs

If the word B(111) becomes 110, the syndromes SPB and SQ3 become 1. The erroneous bit can be located with the syndromes in the way like a crossword puzzle. The problem of this method is that a syndrome is incapable to detect errors when the number of erroneous bits on the same row or column is even.

Word	(1)	(2)	(3)	Parity PP	Syndrome SP
A	1	0	1	0	0
B	1	1	1 → 0	1	1 SPB
Parity PQ	0	1	0	1	0
Syndrome SQ	0	0	1	0	

SQ3

0 : Erroneous bit

Fig. 41 "1"-syndromes Generated From an Erroneous Bit

c) Error correction

The erroneous word B can be corrected by adding the 1's of the same unit on the B and SQ rows as shown in Fig. 42. Even if only one bit is erroneous, the whole bits of the word B are added to their syndromes Q.

The erroneous word is replaced with the corrected word. No correction is required when parity bits only are erroneous. If the B has two erroneous bits, SPB becomes 0 although two bits of Syndrome SQ becomes 1's. Then erroneous word location and correction becomes impossible.

Erroneous word B	1	1	0	← Erroneous bit
Syndrome Q	⊕ 0	0	1	
Corrected word B	1	1	1	

Fig. 42 Erroneous Word Correction

Example 2: Block Error Detection/Correction 1

Word	Binary Code	Separated to 3 blocks :	(1)	(2)	(3)
A	1 1 1 0 0 0 0 1 0	→	1 1 1	0 0 0	0 1 0
B	0 1 1 1 1 1 1 0 1	→	0 1 1	1 1 1	1 0 1

The method of error detection and correction is the same even if each bit of Example 1 are substituted by a group of bits. In this example, the 9-bit words are separated into three 3-bit blocks. Then, each syndrome block also has three bits as shown in Fig. 43. Here, the bits in each block have been aligned diagonally for the convenience of explanation. When generating parities and syndromes, the same significant bits of blocks are added one by one.

a) In case no error exists:

If there is no error, all syndromes become 0.

b) In case one bit is erroneous:

If the bit B₂₁ shifts from 1 to 0, SPB₁ and SQ₂₁ shift to 1. The erroneous bit, then, can be located as a crossword puzzle and corrected by adding the word B and Syndrome SQ.

c) In case two bits on the same check string are erroneous:

If even number of bits, B₁₂ and B₃₂, are erroneous the check bit SPB₂ is incapable of detecting the errors because the total of 1's on the check string SPB₂ is even although SQ₁₂ and SQ₃₂ become 1's. SQ₁₂ and SQ₃₂ thus are incapable of locating the erroneous word.

d) In case three erroneous bits are on two check strings:

If B₁₂, B₂₁ and B₃₂ are erroneous simultaneously, erroneous B₂₁ is located by SPB₁ and SQ₂₁ although the other two erroneous bits are undetectable by SPB₂. The whole errors are then corrected by adding all bits of the word B and SQ as Fig. 44:

As the number of bits in a block increases, the number of bit combinations also increases, thereby increasing the possibility of detecting errors. The number of bits in a block, however, is limited by the processor's capacity.

Word	(1)	(2)	(3)	Parity PP	Syndrome SP
A	1 1 1	0 0 0	0 1 0	1 0 1	0 0 0
B	0 1 1	1 1 1	1 1 1	0 0 1	0 1 0
Parity PQ	1 0 0	1 1 1	1 1 1	1 0 0	0 0 0
Syndrome SQ	0 0 0	0 0 0	0 0 0	0 0 0	

SQ₁₂
SQ₂₁
SQ₃₂
SPB₁
SPB₂

When there are errors, some syndromes become 1's.

Fig. 43 Error Detection of Words Consisting of Blocks

Erroneous word B	0	0	1	0	1	1	1	1
Syndrome Q	⊕ 0	1	0	1	0	0	0	1
Corrected word B	0	1	1	1	1	1	0	1

Fig. 44 Correction of the Erroneous Word B

Two words correction is impossible by this method. The following example, however, makes it possible.

Example 3: Block Error Detection/Correction 2

Higher correctability is required if two blocks on the same row or column drop out. Assume that data are arranged as Fig. 45a, and each block consists of 8-bit information and 4-bit parity word and is capable of detecting its own error, and each P and Q parity string is capable of correcting one block. The P and Q parity and syndrome blocks are produced in the same way as Example 2.

a) In case B1 is erroneous:

If there are erroneous bits in B1, the error is detected by B1's own parity. This time at least one bit each of syndromes SP1 and SQ1 becomes 1. The B1 is corrected by Modulo-2 addition with SP1 in the same way as Example 2 leaving SQ1 unused because B1's errors are detected by B1 itself and SQ1 is not necessary.

b) In case B1 and B2 are erroneous:

If B1 and B2 are erroneous, they are corrected by SQ1 and SQ2 strings respectively because two-block correction by SP1 is impossible.

c) In case B1, B2 and B6 are erroneous:

If B1, B2 and B6 are erroneous, SQ2 string first corrects B2. SP1 then corrects B1 because B2 has been corrected and there is only one erroneous block on the SP1 row. SP2 string then corrects B6.

e) Delaying even-numbered blocks by one block:

When even numbered information blocks are delayed by one block, the column strings are crooked as shown by dotted line in Fig. 46.

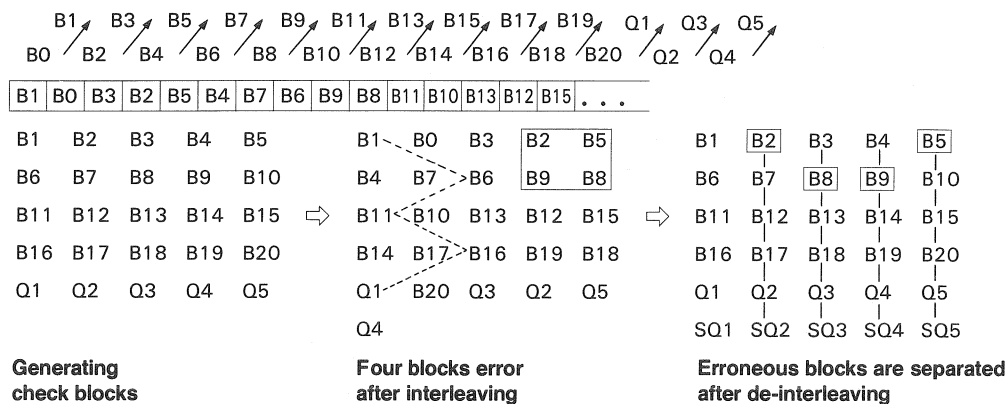


Fig. 46 Crooked SQ Strings by Interleaving

If the adjoining four blocks, B2, B5, B9 and B8 become erroneous after interleaving, they are separated after de-interleaving and become correctable because each of them becomes only one erroneous block on a check string. Refer to Fig. 12.

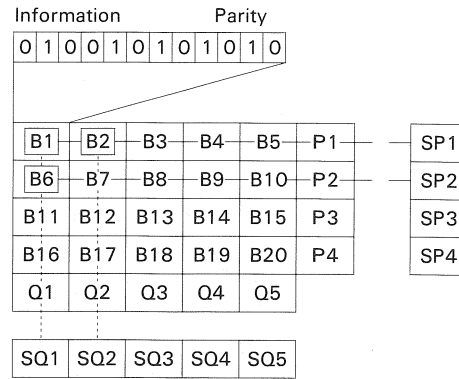


Fig. 45a Detection and Correction of Chained Codes

Erroneous block B1	0	1	1	0	0	0	1	1	0	1	0
Syndrome SP1	⊕	0	0	1	0	1	0	0	1	0	0
Corrected B1	0	1	0	0	1	0	1	0	1	0	1

Fig. 45b Block Correction

d) If B1, B2, B6 and B7 are erroneous, correction becomes impossible by this method.

To avoid continuous block errors, interleaving methods have been introduced. The simplest interleaving is performed as below.

Example 4: Block Correction by Cross-interleave

In Fig. 47, the C1 and C2 decoders are in charge of detecting and correcting errors on each string. C1 and C2 are capable of correcting one and two symbols respectively.

If S13 is erroneous, C1-Q16 corrects it. If S13 and S14 are erroneous, C1Q16 and C1Q20 correct them. If S13 and S16 are erroneous, C2P12 and C2P16 correct them. If S13, S14, S16 and S17 are erroneous, C2P12 and C2P16 correct them by using C1s' pointers. If there are more errors on the P12 and P16 strings, the correction becomes impossible.

The CD system employs more powerful decoders as discussed in page 71. C1 and C2 decoders in the CD system only correct two and three symbols respectively to avoid unreliable correction although they are capable of correcting more symbols. This method is suitable for correcting concentrated burst errors.

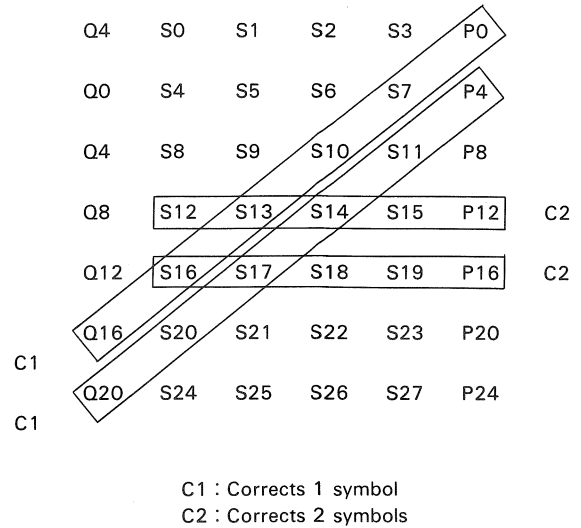


Fig. 47 Parity check by Cross-interleaving

Example 5: Detection with Cyclic Redundancy Check Codes (CRCC)

The detecting and correcting capability increases greatly if each word block has a CRCC parity word. This word is not a product of simple modulo-2 addition but is a residual produced by dividing an information code with a certain

number called generating polynomial. In Fig. 48, horizontal parities have been superseded by CRCCs. The method of detection and correction are basically the same as Example 1 and 2. Detection in each block, however, is more complicated.

Block	Information	CRCC
B1	0 1 0 x 1 x x . .	1 0 1 0
B2
B3
Parity Q
Syndrome Q	0 0 0 1 0 1 1 . .	0 0 0 0

← Erroneous block
} Reproduced data

Fig. 48 Block Detection Employing CRCCs

In this case the erroneous B1 can be corrected by adding with the Syndrome Q although the horizontal check codes have not been produced by Modulo-2 addition.

$$B1 = B2 \oplus B3 \oplus PQ \oplus SQ = \boxed{B1'} \oplus SQ \quad (B1' : \text{erroneous } B1)$$

Example 6: Division Residual As a CRCC Parity Word

Let's see how the above CRCC is generated.

Information word: 110010

Parity word: 3 bits

The decimal number 1984 can be expressed by weighting its units with different powers as follows:

$$1984 = 1 \times 10^3 + 9 \times 10^2 + 8 \times 10^1 + 4 \times 10^0$$

a) Encoding

If the parity word is 3-bit long, the divider is made of 4 bits, and the information number is shifted up by 3 bits to make a space for the parity word. Shifting the information word does not affect the result of decoding. In this example, 1001

In the same way, the binary number 1001 is equal to:

$$1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$$

This can be represented by the following polynomial (a kind of mathematical expression):

$$x^3 + 1$$

has been selected as the divider called generating polynomial. The residue, 100, is employed as the CRCC parity code and is inserted after the information word when recording. Fig. 49 shows how the word is divided.

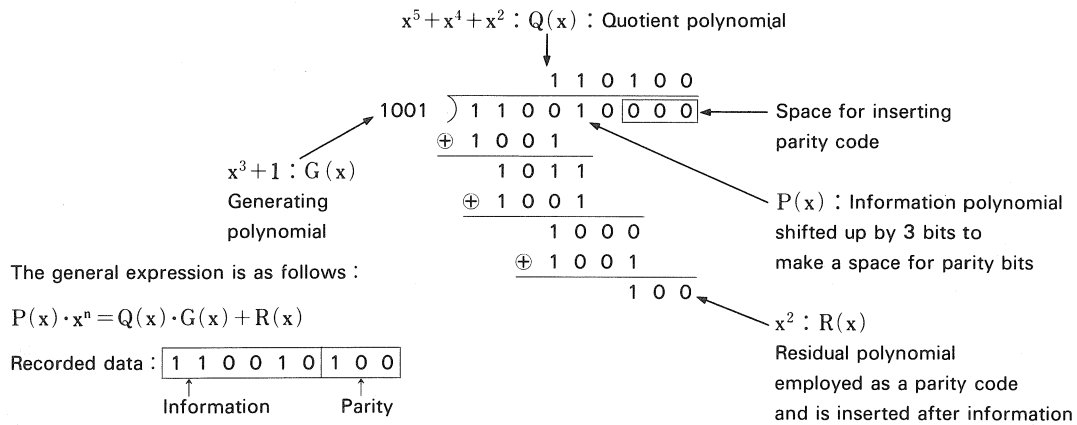


Fig. 49. Dividing an Information Polynomial

b) Decoding

If no error occurs, the reproduced data including the parity word can be divided by the same polynomial (1001).

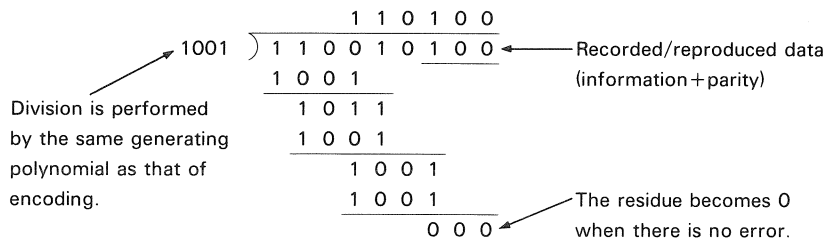


Fig. 50a Zero Residue When No Error Found

If there is an error or errors in the reproduced data, the division generates a residue. Parity words are erased after decoding. The following example has an error at the 2SB and a residue 10.

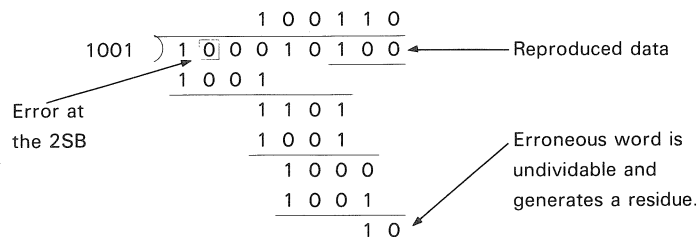


Fig. 50b Error Detection When 2SB Is Erroneous

Example 7: Read Solomon code

The CD system employs a complex double check and interleaving method.

Recorded data	
Information words	Parity words
A 0 0 1	P 1 1 1
B 1 0 1	Q 1 1 0
C 0 1 1	
D 1 0 0	

P and Q are produced by solving two simultaneous equations shown below. The words are simply added in the same way as in the Examples 1 and 2 in the first equation. They are weighted by different power from each other before modulo-2 addition in the second equation.

$$\begin{cases}
 A \oplus B \oplus C \oplus D \oplus P \oplus Q = 0 \\
 \alpha^6 A \oplus \alpha^5 B \oplus \alpha^4 C \oplus \alpha^3 D \oplus \alpha^2 P \oplus \alpha Q = 0
 \end{cases}$$

$$\begin{cases}
 P = \alpha A \oplus \alpha^2 B \oplus \alpha^5 C \oplus \alpha^3 D \\
 Q = \alpha^3 A \oplus \alpha^6 B \oplus \alpha^4 C \oplus \alpha D
 \end{cases}$$

Provided that :

$$\begin{aligned}
 \alpha &= (0\ 1\ 0) \\
 \alpha^2 &= (1\ 0\ 0) \\
 \alpha^3 &= (0\ 1\ 1) \\
 \alpha^4 &= (1\ 1\ 0) \\
 \alpha^5 &= (1\ 1\ 1) \\
 \alpha^6 &= (1\ 0\ 1) \\
 1 = \alpha^7 &= (0\ 0\ 1) \\
 0 &= (0\ 0\ 0)
 \end{aligned}$$

A' ~ Q': Reproduced word
 EA ~ EQ: Error of each word
 α ~ 0: Weighting constant

Syndromes are produced by calculating the following equations:

$$\begin{cases}
 S_1 = A' \oplus B' \oplus C' \oplus D' \oplus P' \oplus Q' \\
 \quad = E_A \oplus E_B \oplus E_C \oplus E_D \oplus E_P \oplus E_Q \\
 S_2 = \alpha^6 A' \oplus \alpha^5 B' \oplus \alpha^4 C' \oplus \alpha^3 D' \oplus \alpha^2 P' \oplus \alpha Q' \\
 \quad = \alpha^6 E_A \oplus \alpha^5 E_B \oplus \alpha^4 E_C \oplus \alpha^3 E_D \oplus \alpha^2 E_P \oplus \alpha E_Q
 \end{cases}$$

If there is no error,
 $S_1 = S_2 = 0$

If the word A is erroneous,
 $S_1 = E_A, \quad S_2 = \alpha^6 S_1$

The erroneous word can be known by the difference of weighting between S_1 and S_2 .

The above complicated calculation is automatically performed by a specially designed IC. For further details, please refer to the books on digital recording or digital communication.

Q & A

Dynamic Range and Signal-to-Noise Ratio

What is the difference between Dynamic Range and Signal-to-Noise ratio (S/N)?

Dynamic Range: Difference between the overload level and the minimum acceptable signal level in a system. Generally distortion in audio equipment increases rapidly at the overload level when the input level is gradually increased, and the signal is masked by noise and becomes unmeasurable at the minimum acceptable signal level when the input signal is gradually decreased. The comparison is made in volts, watts or Sound Pressure Level (SPL; 0 dB is 0.0002 μ Bar or the lowest audible level). The result is expressed in dB. In audio systems, the value shows the ability to reproduce both quiet and loud sounds. The larger the figure, the better. The dynamic range of conventional recording systems has been limited to 70 dB. The new digital audio systems, such as the Compact Disc system, have achieved 90 dB. Refer to "Troubleshooting Power Amplifiers," Supplement to TUNING FORK. With an audio system, ideally all sounds from the weakest to the strongest should be reproduced at levels equal to the original sound source. The maximum audible level is an SPL of 120 dB. The SPLs in our daily life are listed below.

When you try to enjoy a large volume of sound, such as that of a jet plane, with a low-power amplifier, the output is clipped and distorted, and the loudness is limited. Even if the amplifier is powerful, the speaker's maximum input power may be insufficient and may cause clipping distortion. On the other hand, very weak sound may be masked by noise generated in the audio system if the dynamic range of the system is narrow. All peripheral equipment should have the property of wide dynamic range. If the maximum SPL of reproduced sound and that of noise (or unwanted sound components) of a playback system are 100 dB and 30 dB respectively, the dynamic range of the system is 70 dB ($100 - 30 = 70$), or 20 dB narrower than that of the Compact Disc. The noise component generated in a playback system can be measured without input signal.

without input signal.

dB	SOUND SOURCE
175	Space rocket
160	Wind tunnel
140	Jet plane taking off
130	Machine gun
120	Propeller plane taking off
100	Subway train
90	Rivet hammer (20 m distance)
80	Vacuum cleaner
70	Crowded street
60	Conversation (1 m)
50	Quiet restaurant
40	Residential area at midnight
30	Movie theater without audience
20	Whispering (2 m)
10	Breathing
0	Lowest audible level (0.0002 μ Bar)

Table 1 Dynamic Range

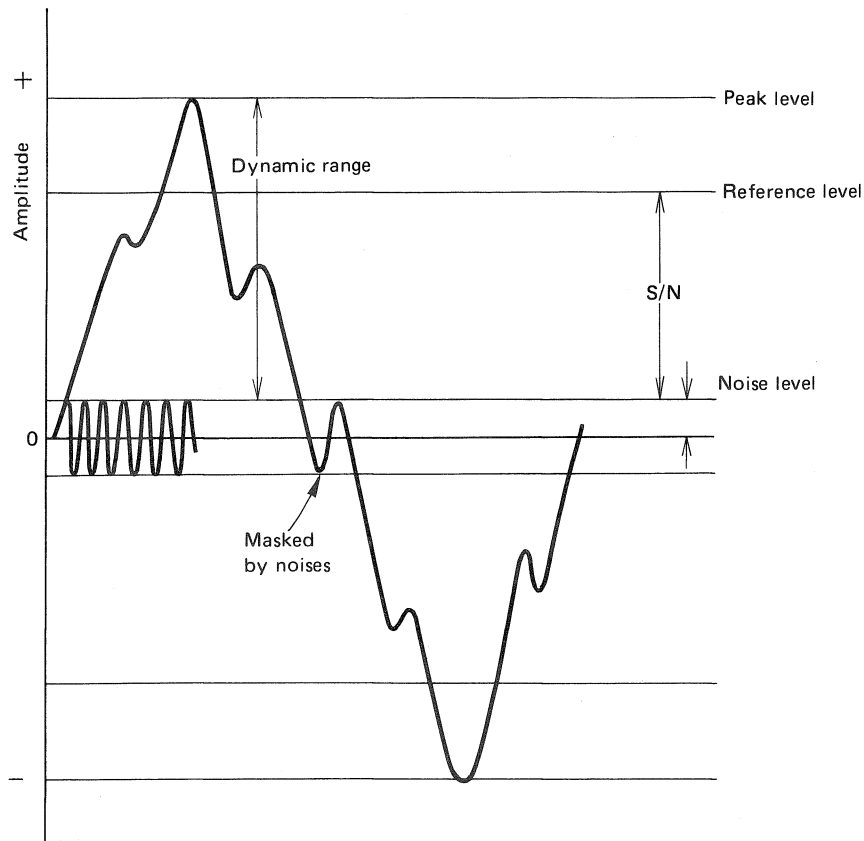


Fig. 1 Dynamic Range and S/N in Amplitude

The necessary dynamic range of a playback system also depends on that of the program source. To reproduce the sound of jet planes and that of a mosquito, a system having a dynamic range of more than 120 dB is required. At the moment, no system has such a wide range; 90 dB is fully wide enough for enjoying music.

Signal-to-noise ratio (S/N): Ratio of the magnitude of a reference signal to that of the noise generated or added in the system. A reference input is required for measuring S/N whereas no reference input is required for measuring dynamic range. The noise level is weighted with a low-pass filter before measuring. The problem in measuring S/N is that reference level, input/output impedance, and the weighting characteristics differ by categories and standards. Even comparing S/N values of models of the same categories does not mean much unless reference level and measuring conditions are equal. Generally S/N is narrower than dynamic range because, as mentioned, S/N is measured with input of a reference level whereas dynamic range is measured with the maximum input level, which is usually higher than the reference.

Reference level of measuring S/N: Turntables: The reference level (0 dB) for turntables is the level obtainable when a 1-kHz signal (5 cm/s horizontal) on a standard test disc is reproduced. The maximum level of the sound reproduced by a turntable depends on the compliance of the cartridge and is about 15 dB higher than the reproduced sound level measured with a reference input. You will see that the dynamic range of a turntable is always larger than S/N in dB.

Tape Deck: There are several methods for measuring the S/N of tape decks. By the DIN method, the recording signal is 333 Hz, and its level shall be at the point where distortion of the third harmonic of the output is 3%. The characteristic of the weighting filter for tape decks differs from that of turntables. The reference level of 250 nWb/m is used by DIN. Refer to TUNING FORK No. 5.

Tuner: The test input signal is 80 dB μ V. A tuner's S/N is the ratio of its output level for an input signal under stipulated modulation to that for an input signal under no modulation. Refer to TUNING FORK No. 3.

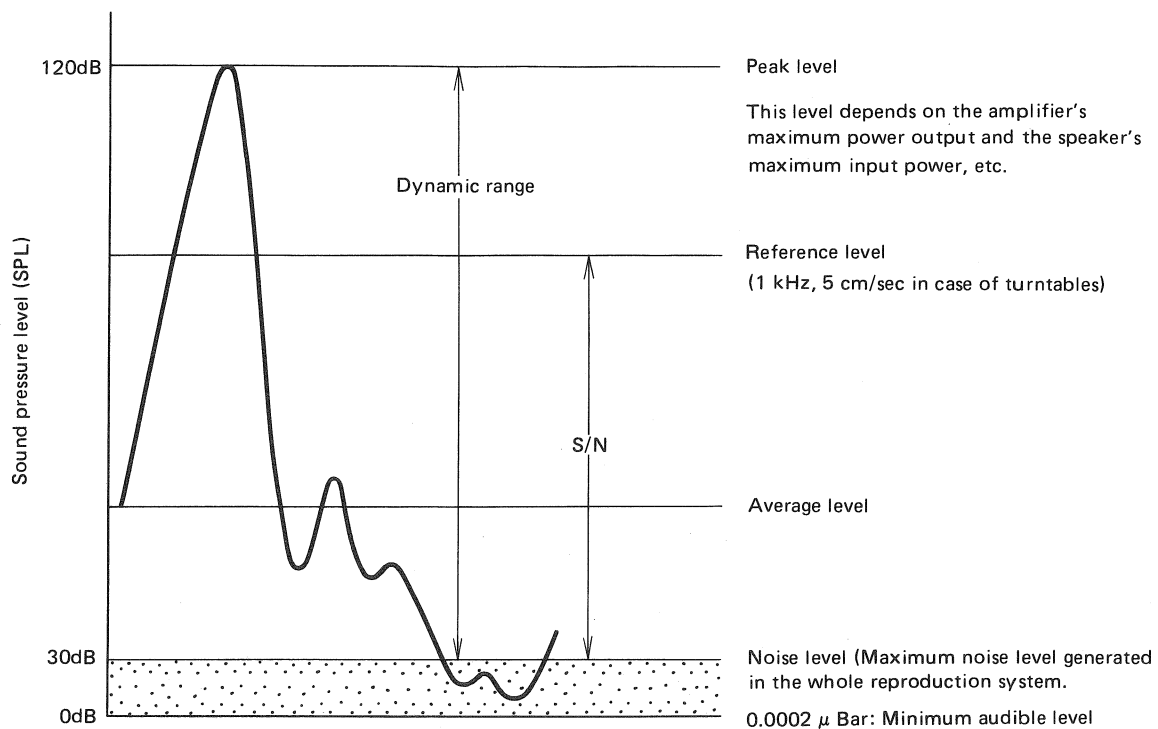


Fig. 2 Dynamic Range and S/N in SPL

Amplifier: There are three popular standards: IHF, EIA, and DIN. Under DIN, the standard input is 5 mV (MM/PHONO) or 0.5V (AUX, TUNER, TAPE), and the standard output is from 50 mW to rated output per channel. The terminating resistors and capacitor are:

MM: 2.2 k Ω ,
 AUX: 47 k Ω +250 pF

As far as amplifiers are concerned, the values of dynamic range and S/N are equal.

As seen above, measuring standards differ between dynamic range and S/N. Exact comparison of the difference of S/N itself among items in the same category is impossible unless the measuring method is the same. So use the dB values of Dynamic Range and S/N, only for rough comparison.

MEMO

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